HYBRID COMPUTER SYSTEM
REQUEST FOR PROPOSAL

JANUARY 1966

Lockheed

MISSILES & SPACE COMPANY

A GROUP DIVISION OF LOCKHEED AIRCRAFT CORPORATION

SUNNYVALE, CALIFORNIA

LOCKHEED MISSILES & SPACE COMPANY

HYBRID COMPUTER

ANALOG SECTION

INSTRUCTIONS TO BIDDERS

Bidders must respond to all numbered items. If Bidder wishes to take exception to any requirement, he may do so provided he includes a section of his proposal labled EXCEPTIONS and clearly indicates which item or items where he has taken an exception.

Bidders are to provide price breakdowns for all two digit numbered items in Sections 1, 2, 3, and 4.

Bidders are to provide their own guaranteed specifications whice are called for in Section 5, and must provide the information on the forms provided in Section 10. Other specification information will be considered only if the Method of Measurement is clearly defined. It is requested that if other specification information is included, that the formats in Section 10 be used where applicable.

Bidders proposals must contain a clear description of all aspects of their computer systems and peripheral equipment. It is requested that where possible the descriptions follow the outline in Sections 1 through 4.

Additional options will be considered if bidder clearly shows that there will be no reduction in computing capability and what advantage the option would provide to Lockheed Missiles and Space Company.

Any computing element proposed must be available for demonstration and testing under system operating conditions at any time after receipt of proposals.

STATEMENT OF REQUIREMENTS:

The intent of this procurement is to purchase five identical analog computer systems containing all solid state computing components of the highest static accuracy and best dynamic performance.

1.0 Minimum Complement of computing components for each of five analog computer systems:

1.1 Analog computer console and cabinets completely wired with all necessary power supplies and operating controls.

1.1.1 Console shall contain an overload indicator system.

1.1.2 Console shall contain an oscilloscope display system.

1.1.3 Console shall contain a Rate Test feature.

1.1.4 Console shall contain a temperature controlled capacitor oven.

1.1.5 Console shall contain a shielded analog patch bay.

1.1.6 Console shall contain an Electronic Digital VoltMeter.

1.1.7 Console shall contain a transistor VoltMeter.

1.1.8 Console shall contain a reference voltage system. Voltage may be any level. The reference system will be capable of being slaved to any one of the four other consoles.

1.1.9 Console shall contain a reference divider system capable of local and remote operation. Remote mode must be capable of accepting inputs from a digital computer or an automatic set up device.

1.1.10 Console shall have a mode control system capable of local and remote operation. Remote mode must be capable of accepting inputs from any other analog computer, either one of two digital computers, or an automatic set up device.

1.1.11 Console shall contain an addressing system that can select any computing component. Addressing system must be capable of local and remote operation. Remote mode must be capable of accepting address from either one of two digital computers or an automatic set up device.

1.1.12 Console shall contain a power supply monitor system capable of reading all the power supplies in the analog computer system on the EDVM, TVM or oscilloscope.

1.2 60 Integrators

1.2.1 Each capable of summer, integrator or high gain operation.

1.2.2 Each having the capability of at least six input resistors, 3 providing gains of one, and 3 providing gains of 10 when a normal feedback resistor is used.

1.2.3 Each having the capability of a selection of an integration time constant of one second, one hundred milliseconds, ten milliseconds and one millisecond, when used with a standard gain of one input resistor.

1.2.4 One third or more of the integrators should have the capability of selecting an integration time constant of ten seconds when used with a standard gain of one input resistor.

1.2.5 Each having the capability of electronic switching mode control for Initial Condition, Hold and Operate modes.

1.2.6 Each having the capability of independent mode control for Initial Condition, Hold, and Operate modes.

1.2.7 Each having the capability of holding the input network's summing junction to zero volts in the Pot Set and Initial Condition modes.

1.2.8 Each having the initial condition summing junction available on the patchboard.

1.2.9 Each having the capability of having the initial rate from the input summing junction available for readout in the initial condition and static check modes.

1.3 60 Summers

1.3.1 Each capable of summer or high gain operation.

1.3.2 Each having the capability of at least six input resistors, 3 providing gains of one, and 3 providing gains of 10 when a normal feedback resistor is used.

1.3.3 Each having the capability of holding the input network's summing junction to zero volts in the Pot Set mode.

1.4 240 Potentiometers

1.4.1 20 Potentiometers are to be three terminal manual set with a ground connection to be made by a bottle plug.

1.4.2 All potentiometers except the three terminal are to be servo set.

1.4.3 All potentiometers except the three terminal are to be phase shift compensated.

1.5 90 Electronic Multipliers

1.5.1 Approximately one half of the multipliers should be class 2, accepting +x and +y from low impedances source and providing a low impedance output.

1.5.2 Approximately one forth of the multipliers should be class 3, accepting +x and $\pm$y from a low impedance source and providing a low impedance output, or accepting +x and +y from a low impedance source and providing a current output. The patchboard configuration should be such that the programmer has the option for either mode of class 3 operation as well as providing for division and square root modes.

1.5.3 Approximately one forth of the multipliers will normally be associated with the Electronic Resolvers, but will be available as multipliers as a programmer option when resolvers are not used.

1.6 6 Electronic Resolvers

1.6.1 Each resolver shall be capable of polar to rectangular conversion of 2 two dimensional vectors.

1.6.2 Each resolver shall be capable of rectangular to polar conversion of a two dimensional vector.

1.6.3 Each resolver shall be capable of continuous resolution in both the polar to rectangular and rectangular to polar modes.

1.7 24 Stored Program Dioded Function Generators

1.7.1 Each function generator shall be set by a pre-programmed device such as a card, special board, or digital computer.

1.7.2 Each function generator shall have at least ten segments plus a parallax adjustment.

1.7.3 Both the breakpoints and slope shall be adjustable.

1.7.4 Each function generator should be class 1, accepting x from a low impedance source and providing f(x) as a low impedance output.

1.7.5 Pairs of function generators, by a programmer option, may be combined for twenty segment operation.

1.8 30 Feedback Limiters

1.8.1 Each limiter must be adjustable over the entire reference voltage range.

1.8.2 Each limiter shall provide hard limiting for summers and integrators.

1.9 30 Comparators

1.9.1 Each comparator will have its output and complemented output available in the logic area.

1.10 30 Electronic Switches

1.10.1 Each switch shall be capable of being controlled by any logic signal in the logic area.

1.10.2 Each switch shall be capable of switching voltages over the entire reference voltage range.

1.11 24 Relays

1.11.1 Each relay shall be double pole double throw.

1.11.2 Each relay shall be capable of being set by any logic signal in the logic area.

1.12 15 Function Switches

1.12.1 Each function switch shall be single-pole triple throw.

1.13 200 Analog Trunks

1.14 250 Logic Units

1.14.1 A logic unit is defined as a gate, flip flop, one shot, each stage of a shift register, each binary stage of a counter, etc.

1.14.2 Each logic unit will have both true and complemented outputs available.

1.14.3 The logic may be either synchronous or asynchronous, but if the latter, a clock must be available at the patchboard.

1.14.4 The logic board will have at least 100 trunk lines.

1.15 10 Analog Patchboards

1.15.1 Analog patchboards are to provide shielding for patch cords.

1.16 1,000 Analog Patching Elements

1.16.1 Analog patching elements are patch cords, bottle plugs and multiples.

1.16.2 All patching elements are to be shielded.

1.17 10 Logic Patchboards

1.18 500 Logic Patching Elements

1.18.1 Logic patching elements are patch cords, bottle plugs and multiples.

1.19 1 DC to low frequency noise generator.

1.20 1 High frequency noise generator

2.0 Peripheral Equipment:

2.1 15 Eight Channel Strip Chart Recorders

2.1.1 Must be capable of slaving with the analog computer mode control.

2.1.2 Must be capable of operating the analog computer mode control.

2.2 15 X-Y Plotters

2.2.1 Each must be capable of plotting over a 10 x 15 inch range.

2.2.2 Pen operation must be capable of being slaved to the analog computer mode control.

2.3 2 Automatic Set up and Checkout Devices

2.3.1 Must be capable of setting all servo set pots.

2.3.2 Must be capable of reading all computing components.

2.3.3 Must be capable of activating the computer mode control.

2.3.4 Read and store all potsetting in a suitable form for reprogramming the computer.

2.4 1 Analog Patchboard Storage System

2.4.1 Must be capable of holding all of the analog patchboards in a fully wired condition.

2.5 1 Logic Patchboard Storage System

2.5.1 Must be capable of holding all of the logic patchboards in a fully wired condition. Can be incorporated with Item 2.4.

2.6 1 Patch Cord Storage System

2.6.1 Must be capable of holding all of the patch cords, both analog and logic.

2.6.2 Shall be arranged in such a manner to facilitate patching either analog or logic patchboards.

3.0 Spares and Test Equipment:

3.1 1 Test Rack

3.1.1 Capable of testing and calibrating all computing elements to original specifications, operating in the same system environment as the computer system.

3.1.2 Capable of testing and calibrating all logic elements to original specifications, operating in the same system environment as the logic system.

3.1.3 Test rack may use spare computing components to implement the above tests.

3.2 1 Reference Divider System

3.2.1 System must provide two voltages simultaneously, one to be used as an input, the other to be used as a nulling voltage.

3.2.2 System must be capable of dividing reference by .001% steps.

3.2.3 System must have preprogramming capability for selecting standard test and calibration voltages.

3.2.4 System must be portable.

3.3 1 Lot Spare Computing Elements

3.3.1 Shall include EDVM, power supplies, reference, amplifier networks, and approximately one or two percent of the plug in spare components, but at least two of each type of computing element or card.

3.4 1 Lot Spare Parts

3.4.1 Shall include at least two each of each type of resistor, capacitor, diode, transistor and relay that are used in the computer system.

4.0 Options:

4.1 Delete one computer console as described in Item 1.

4.2 Delete 3 eight channel recorders, 3 X-Y plotters as described in Items 2.1 and 2.2

4.3 Delete 1 automatic set up and checkout device as described in Item 2.3.

4.4 Substitute a parallel entry keyboard for both the addressing and reference divider systems.

4.5 Substitute electronic digital attenuators for all of the servo set potentiometers.

5.0 Required Specifications:

5.1 Drift

5.1.1 Arbitrary Electronic Function Generator

5.1.2 Electronic Multiplier

5.1.3 Electronic Sinusoid Generator

5.1.4 Integrator Amplifier

5.1.5 Summing Amplifier

5.1.6 SCI Method of Measurement

5.1.7 Format for results 10.1.

5.2 Error, Total

5.2.1 Electronic Multiplier

5.2.1.1 SCI Method of Measurement

5.2.1.2 Format for results 10.2.1

5.2.2 Combination Amplifier

5.2.2.1 SCI Method of Measurement for Summing Amplifier with the combination amplifier in the summing mode.

5.2.2.2 Format for results 10.2.2

5.2.3 Summing Amplifier

5.2.3.1 SCI Method of Measurement

5.2.3.2 Format for results 10.2.2

5.3 Frequency Response, Amplitude

5.3.1 Combination Amplifier

5.3.1.1 SCI Method of Measurement for amplifier with the combination amplifier in the summing mode.

5.3.2 Summing Amplifier

5.3.2.1 SCI Method of Measurement for amplifier.

5.3.3 Arbitrary Electronic Function Generator

5.3.3.1 SCI Method of Measurement

5.3.4 Electronic Multiplier

5.3.4.1 SCI Method of Measurement

5.3.5 Electronic Sinusoid Generator

5.3.5.1 SCI Method of Measurement

5.3.6 Format for results 10.3.

5.4 Frequency Response, Phase

5.4.1 Combination Amplifier

5.4.1.1 SCI Method of Measurement for amplifier with the combination amplifier in the summer mode.

5.4.2 Summing Amplifier

5.4.2.1 SCI Method of Measurement for amplifier

5.4.3 Arbitrary Electronic Function Generator

5.4.3.1 SCI Method of Measurement

5.4.4 Electronic Multipliers

5.4.4.1 SCI Method of Measurement

5.4.5 Electronic Sinusoid Generator

5.4.5.1 SCI Method of Measurement

5.4.6 Format for results 10.4.

5.5 Noise

5.5.1 Arbitrary Electronic Function Generator

5.5.2 Electronic Multiplier

5.5.3 Electronic Sinusoid Generator

5.5.4 Summing Amplifier

5.5.5 SCI Method of Measurement

5.5.6 Format for results 10.5.

5.6 Recovery Time, Overload

5.6.1 Arbitrary Electronic Function Generator

5.6.2 Electronic Multiplier

5.6.3 Electronic Sinusoid Generator

5.6.4 Summing Amplifier

5.6.5 SCI Method of Measurement

5.6.6 Format for results 10.6.

5.7 Response, Transient

5.7.1 Arbitrary Electronic Function Generator

5.7.2 Electronic Multiplier

5.7.3 Electronic Sinusoid Generator

5.7.4 Summing Amplifier

5.7.5 SCI Method of Measurement

5.7.6 Format for results 10.7.

5.8 Response, Transient, Under Capacitive Loading

5.8.1 Summing Amplifier

5.8.2 SCI Method of Measurement

5.8.3 Format for results 10.8.

5.9 Crosstalk, Patchboard Amplifiers

5.9.1 Method of Measurement 9.1

5.9.2 Format for results 10.9.

5.10 Output Impedance

5.10.1 Combination Amplifiers

5.10.2 Summing Amplifier

5.10.3 Method of Measurement 9.2

5.10.4 Format for results 10.10.

5.11 Velocity Limit

5.11.1 Combination Amplifier

5.11.2 Summing Amplifier

5.11.3 Method of Measurement 9.3

5.11.4 Format for results 10.11

6.0 Computer System's Environmental Requirements:

6.1 Bidders shall submit dimensioned drawings showing the physical size of all consoles, cabinets and peripheral devices. Drawing will indicate the location of airconditioning intakes and exhausts, power cords, and other external cable requirements.

6.2 Bidders shall submit a suggested arrangement of a computer system including the arrangement of the peripheral equipment.

6.3 Bidders will indicate the clearances required for maintenance access to the computer system and the peripheral equipment.

6.4 Bidders shall submit floor loading data for the computer system.

6.5 Bidders shall submit electrical power requirements for computer system and peripheral equipment.

6.6 Bidders shall submit airconditioning requirements for the computer system and peripheral equipment. Data will include the volume and temperature of the intake air and the temperature of the exhaust air.

6.7 Bidders shall submit any additional facility requirements for the installation or operation of the computer systems and peripheral equipment.

7.0 Successful bidder shall provide five (5) copies of maintenance procedures and maintenance manuals for all computing components and peripheral equipment.

8.0 Inspection and Delivery

8.1 Successful bidder shall notify Lockheed Missiles and Space Company at least two weeks in advance of a date for inspection of the computer systems at the bidder's plant.

8.2 Successful bidder shall provide space and test equipment for representatives of Lockheed Missiles and Space Company to inspect and test the computer system prior to shipment.

8.3 Shipment of the computer systems can be made only after successfully meeting specifications. Meeting of specifications is to be determined by Lockheed Missiles and Space Company.

8.4 Shipment is to be F.O.B. Lockheed Missiles and Space Company, Sunnyvale, California.

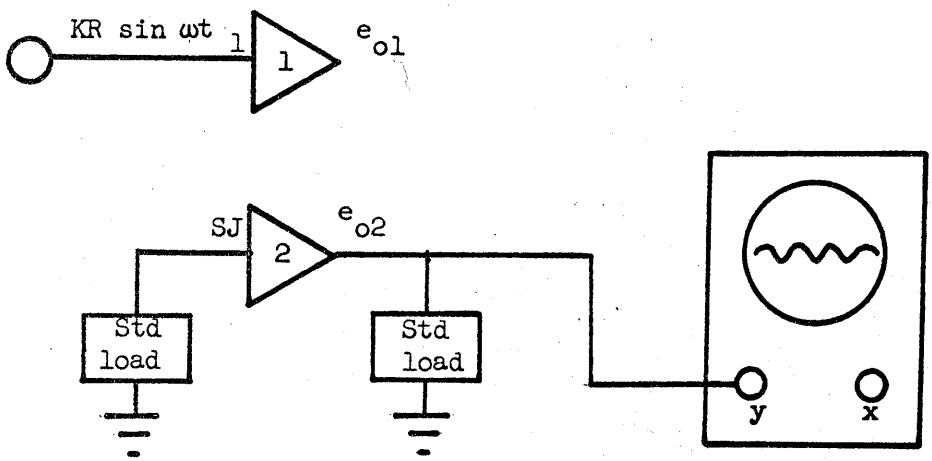
8.5 Bidder shall submit a delivery date based on receipt of purchase order.

8.6 Bidder shall provide a plan to compensate LMSC in the event bidder is unable to meet his delivery date.

9.0 Method of Measurement:

9.1 Cross Talk, Amplifier

The following circuit is recommended for measurement of amplifier cross talk. Worse case results for any combination of amplifiers on the patch-board should be given as the crosstalk specifications.



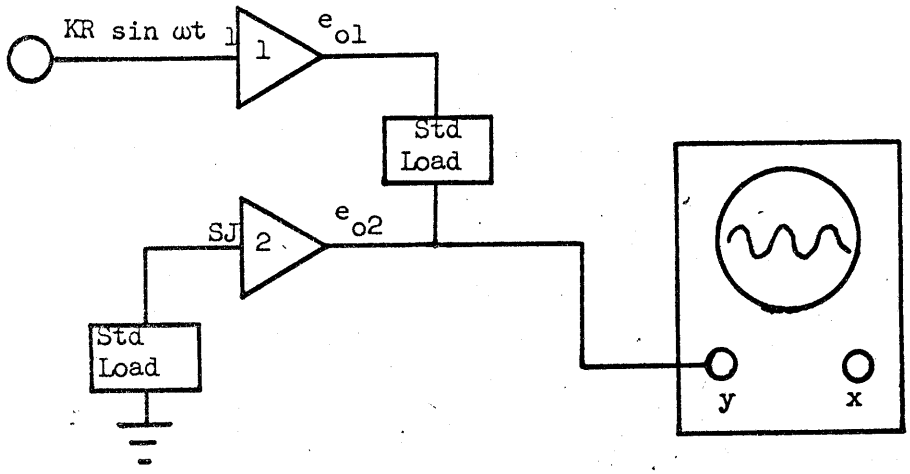
Cross talk ratio = $\frac{e_{o2}}{KR}$

Suggested values of K is 1.0

R = Reference voltage.

9.2 Output Impedance

The following circuit is recommended for measurement of amplifier output impedance.



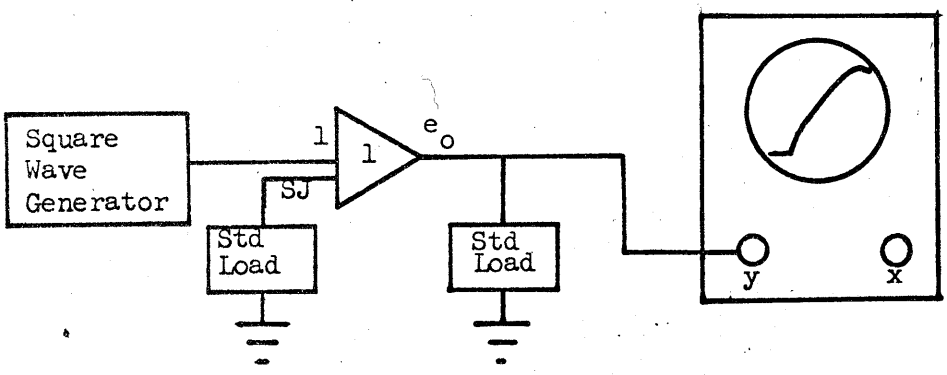
$$\text{Output Impedance} = \frac{e_{o2\ Max}\ R_L}{KR - e_{o2\ Max}}$$

Where R_L is the value of the standard output load in ohms.

Suggested value of K is 1.0.

9.3 Velocity Limit

Velocity limit can be measured by the circuit shown below:



Recommended value of K is 1.0. The frequency of the square wave generator and the time scale of the oscilloscope should be adjusted to give the best resolution of the output slope.

$$\text{Velocity limit} = \frac{.8\ KR}{t_{.9eo} - t_{.1eo}}$$

Where $t_{.9eo}$ is the time required for e_o to reach .9 KR and $t_{.1eo}$ is the time required for e_o to reach .1 KR.

SCI square wave generator may be used.

10.0 Format for Specifications

10.1 Drift

10.1.1 Arbitrary Electronic Function Generator

_____ Microvolts/hour

_____ % R/hour

10.1.2 Electronic Multiplier

_____ Microvolts/hour

_____ %R/hour

10.1.3 Electronic Sinusoid Generator

_____ Microvolts/hour

_____ %R/hour

10.1.4 Integrator Amplifier

10.1.4.1 Hold Mode

_____ Microvolts/second

_____ %R/second

10.1.4.2 Operate Mode

_____ Microvolts/second

_____ %R/second

10.1.5 Summing Amplifier

_____ Microvolts/hour

_____ %R/hour

10.2 See Graphs

10.3 See Graphs

10.4 See Graphs

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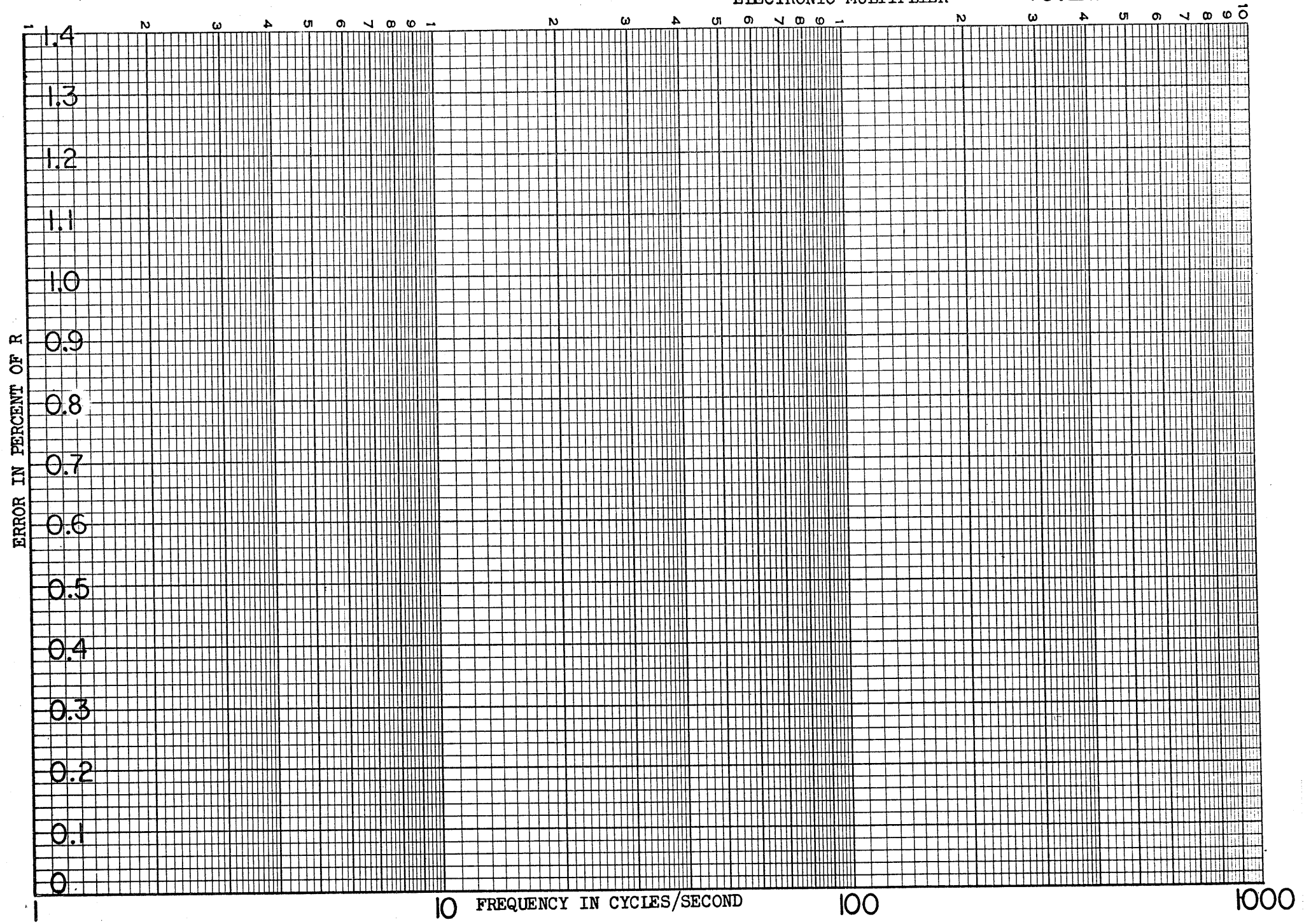
911TR370 SEMI-LOGARITHMIC 3 3⅓" CYCLES

ERROR, TOTAL
ELECTRONIC MULTIPLIER

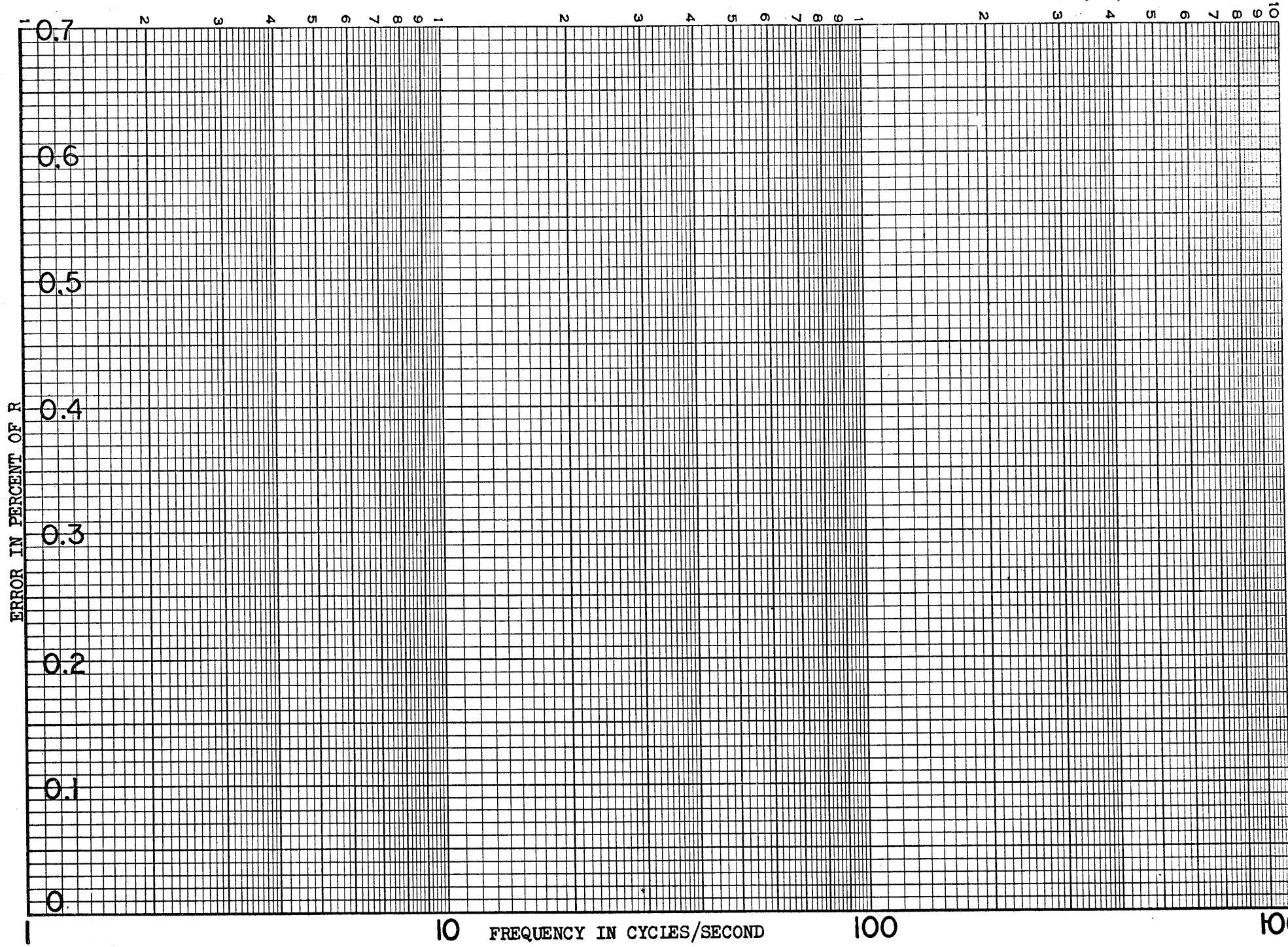
10.2.1



FREDERICK POST COMPANY
311TR370 SEMI-LOGARITHMIC 3 3½" CYCLES

ERROR TOTAL AMPLIFIER

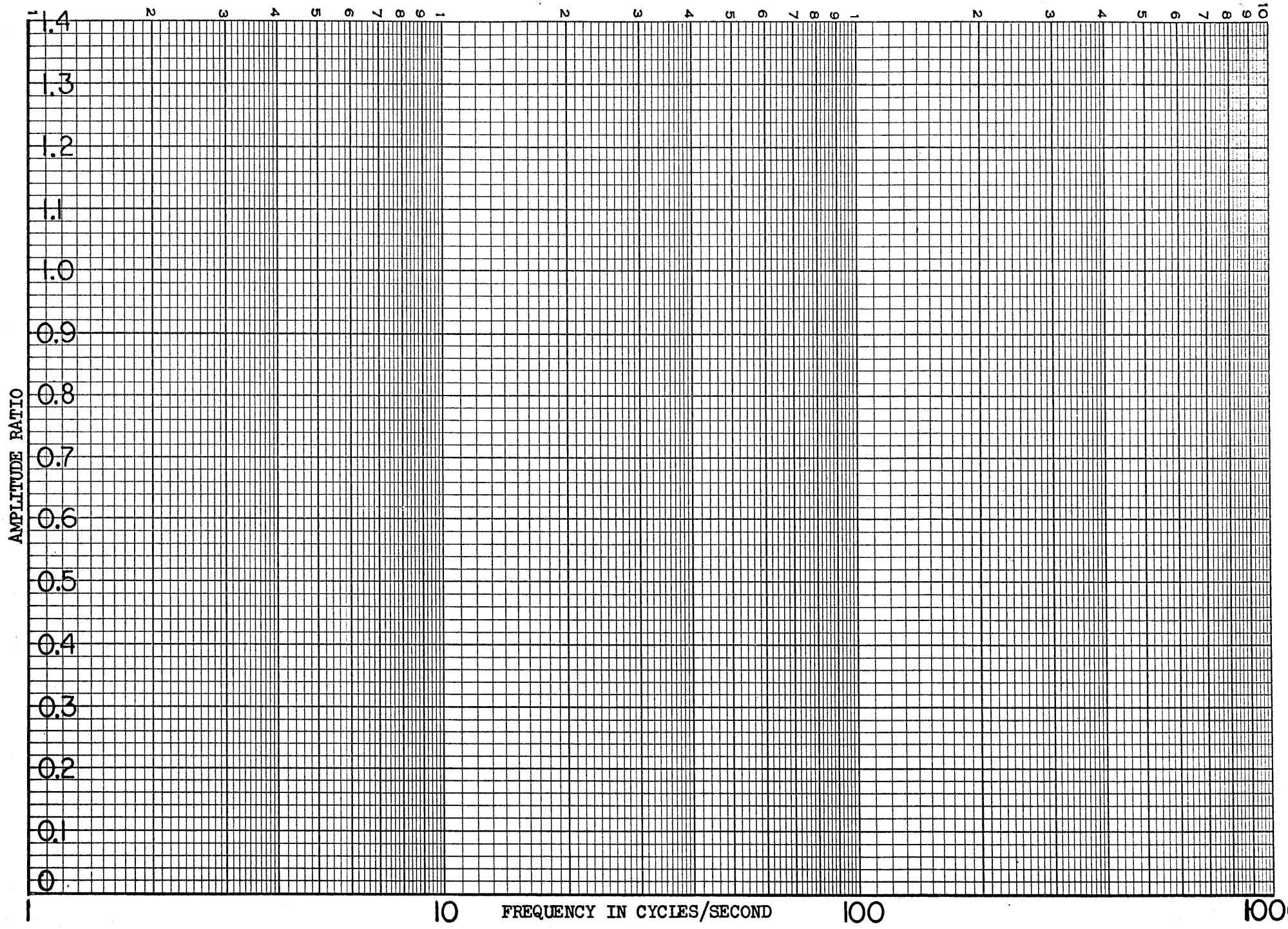
10.2.2



FREDERICK POST COMPANY
311TR370 SEMI-LOGARITHMIC 3 3⅓" CYCLES

FREQUENCY RESPONSE, AMPLITUDE

10.3



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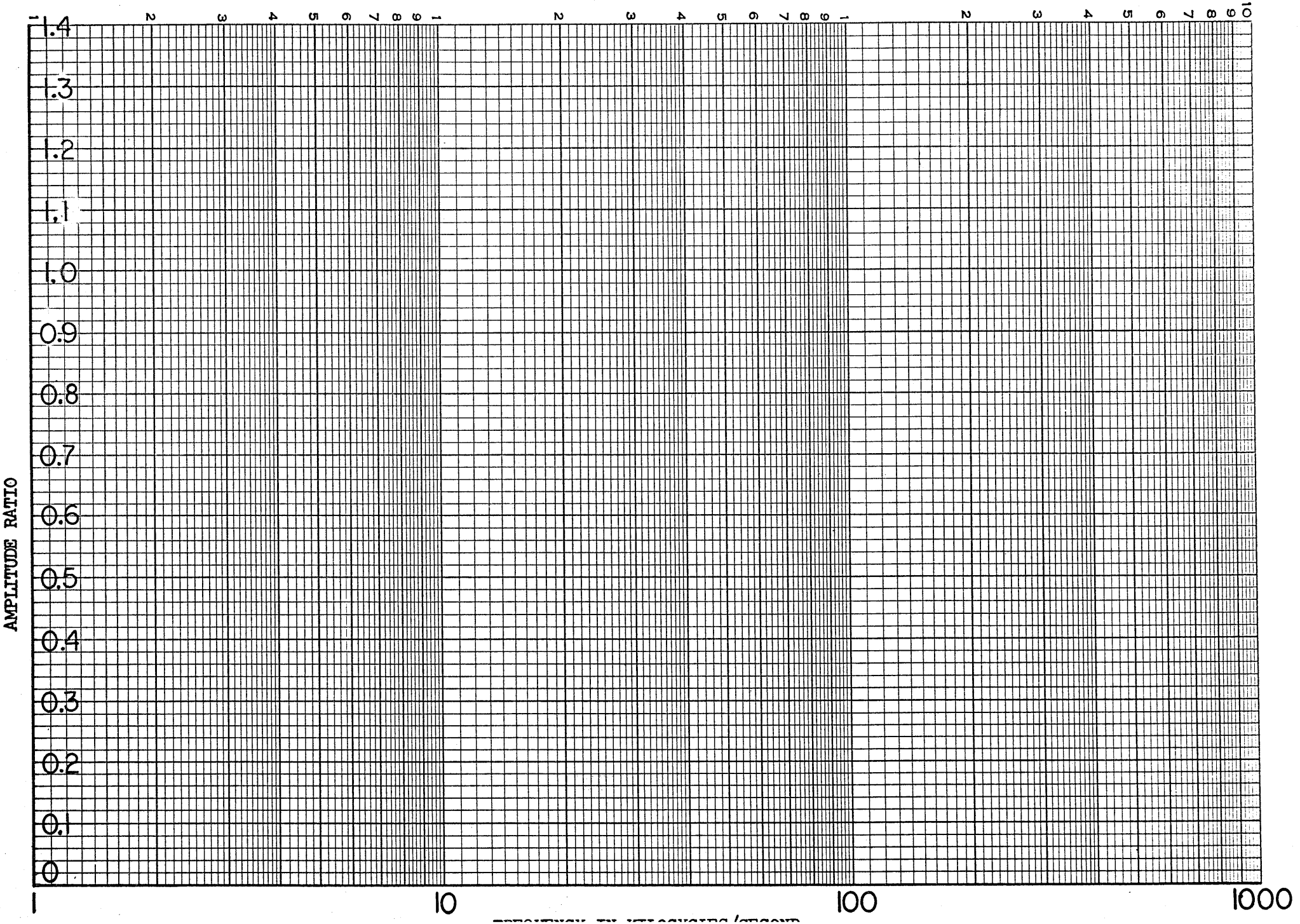
FREQUENCY RESPONSE, AMPLITUDE

10.3



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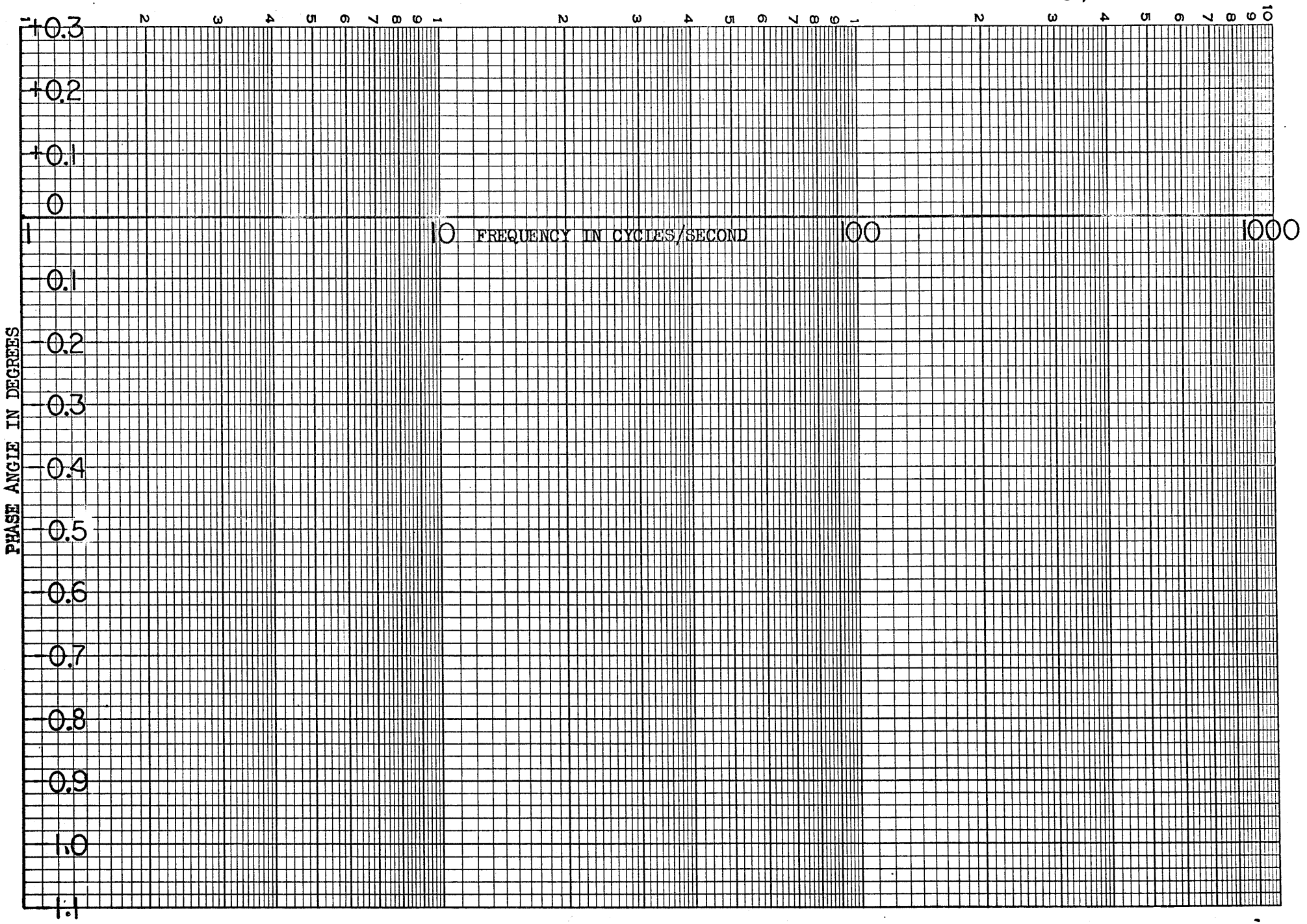
FREQUENCY RESPONSE, PHASE 10,4



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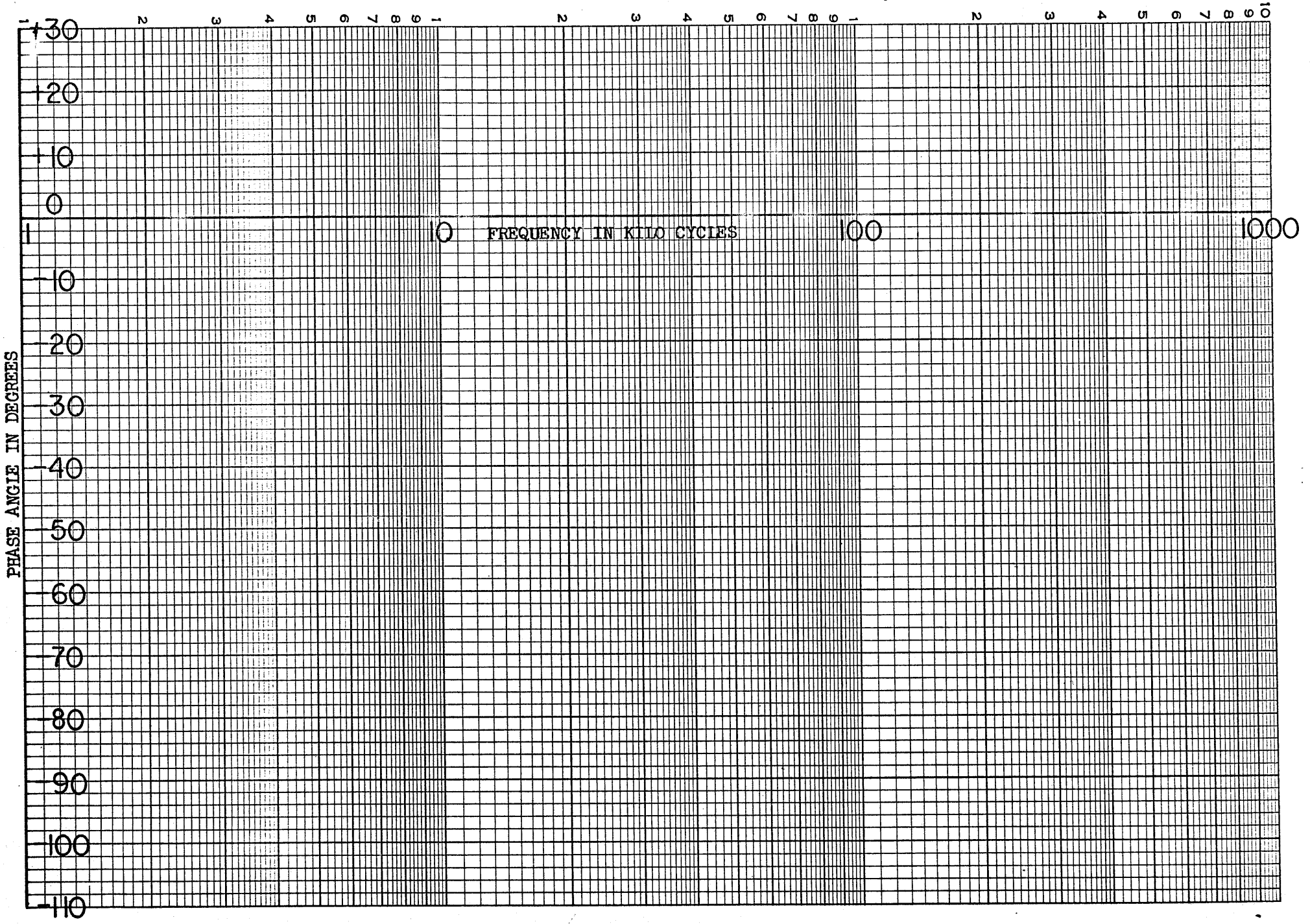
FREQUENCY RESPONSE, PHASE 10.4



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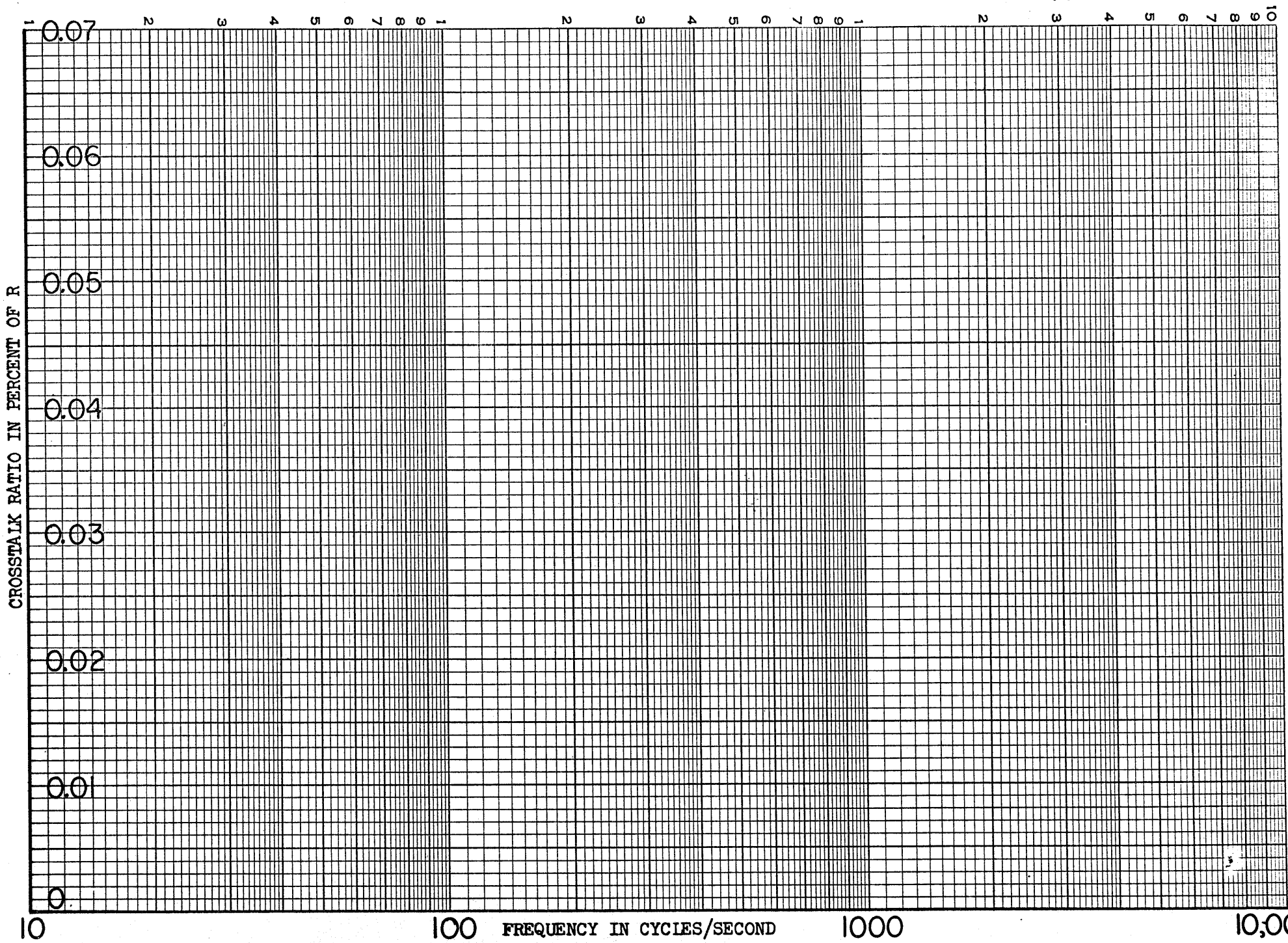
CROSSTALK 10.9



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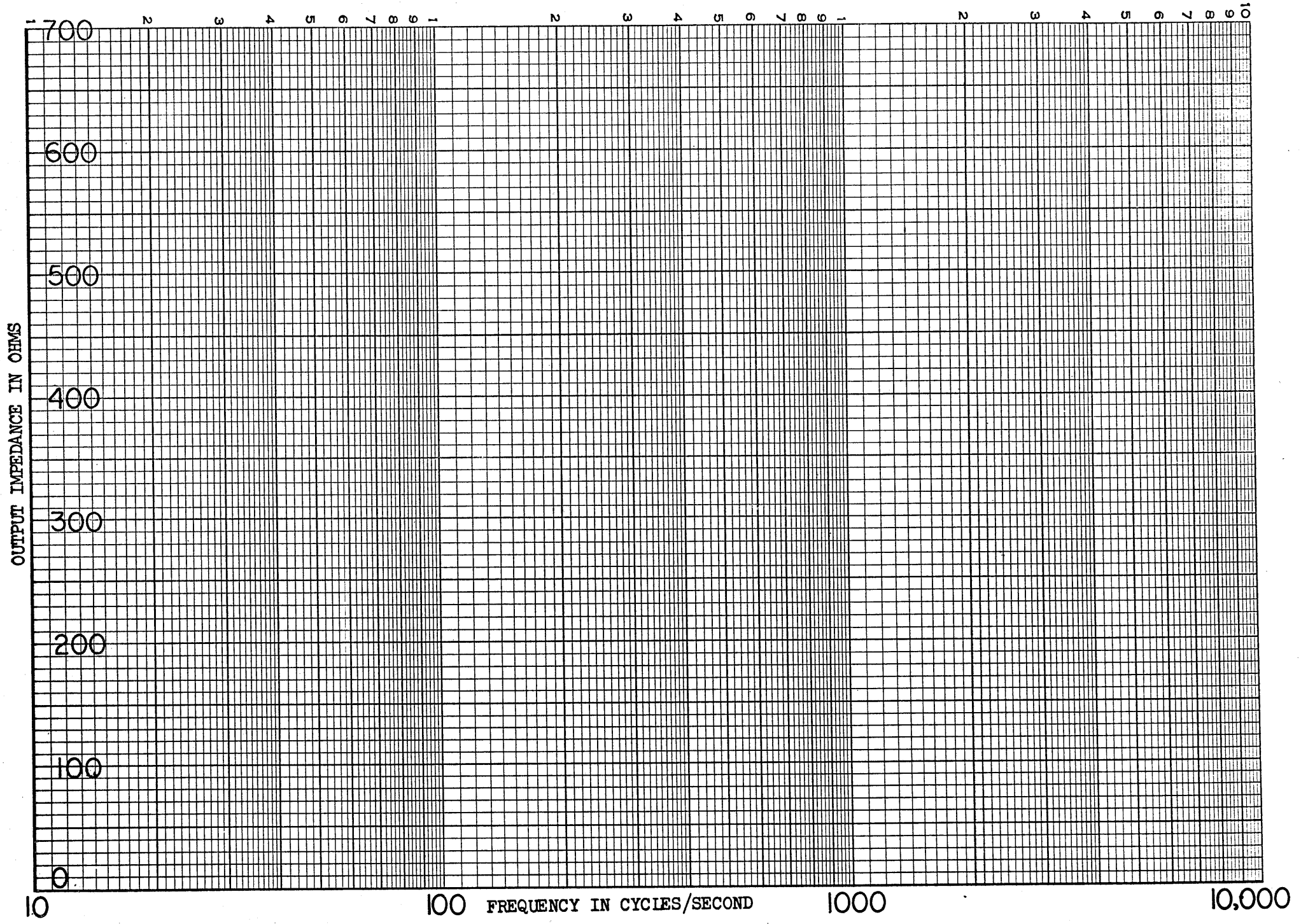
OUTPUT IMPEDANCE

10.10



10.5 Noise

Photo-oscillograms with y-axis calibrations in peak to peak millivolts and as a percentage of R. SCI filter cut off frequencies.

10.6 Recovery Time, Overload

Photo-oscillograms with x-axis calibrations in time.

10.7 Response, Transient

Photo-oscillograms for K equal to 0.1 and 0.8.

10.8 Response, Transient, under Capacitive loading.

Photo-oscillograms.

10.9 See Graphs.

10.10 See Graphs.

10.11 Velocity Limit

Photo-oscillograms with the x-axis calibrated in time and the y-axis calibrated in percent of R. In addition, photo-oscillograms should be marked with the velocity limit value.

LOCKHEED MISSILES AND SPACE COMPANY

HYBRID COMPUTER

INTERFACE SECTION

INDEX

1.0 Title:

Lockheed Missiles and Space Company, Hybrid Computer Interface Section

2.0 Purpose:

The purpose of this request for proposal (RFP) is to set forth the functional description of an interface system to connect the digital and analog computers defined in the following two RFP's:

- Lockheed Missiles and Space Company Hybrid Computer, Digital Section
- Lockheed Missiles and Space Company Hybrid Computer, Analog Section

3.0 General Description:

The proposed interface equipment (Figure 1) shall be installed at LMSC, Sunnyvale, California in Building 181 as a linkage system between analog and digital computers which will be delivered during 1966.

The digital section of the hybrid computing system is described in the RFP entitled LMSC Hybrid Computer, Digital Section. The analog section of the computing system is described in the RFP entitled LMSC Hybrid Computer, Analog Section. The digital section will consist of two medium sized digital computers or their equivalent. The analog section will consist of five analog computers (with general purpose logic units) and two small digital set-up computers.

The proposed linkage equipment will be composed of two identical interface systems denoted in Figure 1 as 'A' and 'B'. Both interface systems will be distinct and independent of each other and capable of simultaneously operating as part of separate hybrid computer simulations.

The proposed linkage system will be flexible in that analog to digital channels and digital to analog channels and general purpose logic not used in one interface subsystem can be used in the other. Each of the two interface systems will have capability for both high accuracy high speed data transmission, and effective control and monitoring of an independent hybrid simulation.

4.0 Interface Philosophy:

4.1 General

The following operational philosophies shall dictate the overall design and construction of the Hybrid Computer interface described in this request.

4.2 Pure Digital Mode

The hybrid interface system shall not interfer nor restrict either of the digital computers from operating in its normal digital mode, independent of the interface and all other computers.

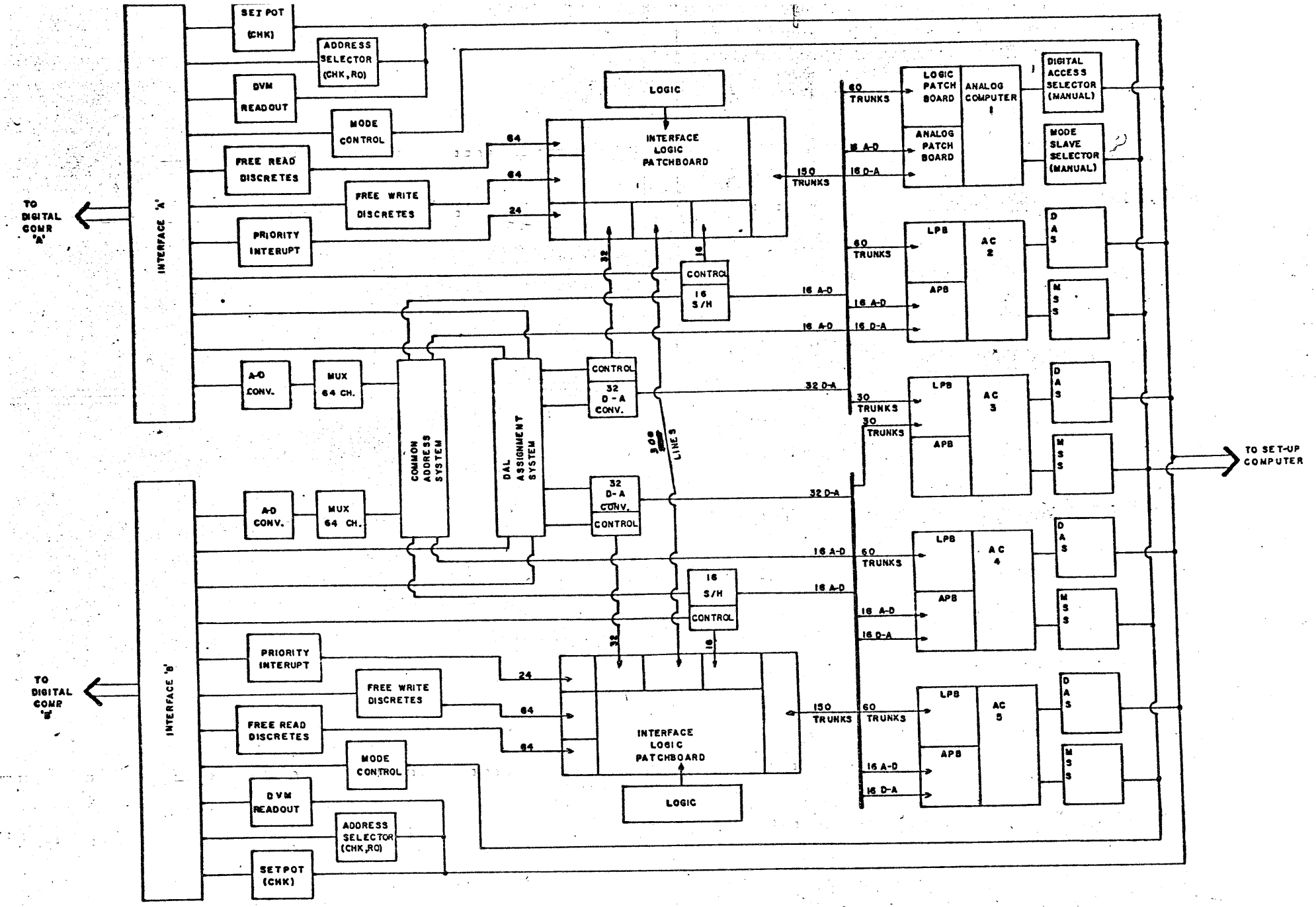


FIGURE I

LMSC HYBRID COMPUTER INTERFACE - FUNCTIONAL BLOCK DIAGRAM

4.3 Pure Analog Mode

The hybrid interface system shall not interfer nor restrict any combination of the analog computers from operating in their normal analog mode, independent of the interface and all other computers.

4.4 Hybrid Mode

The hybrid interface system shall be composed of two identical, distinct, and independent interface systems, 'A' and 'B'. These interface systems shall be constructed such that the following modes of operation can be performed.

4.4.1 Each of the two interface systems shall be designed and constructed such that unused analog-to-digital and digital-to-analog conversion channels (ADC, DAC) and unused general purpose logic in one interface system can be used by the other interface system (See: 5.2.2 and 5.4.11).

4.4.2 Component failure (e.g., power supply, disconnected cable, etc.) in one interface system shall not interfer nor restrict the standard operation of the other interface system. (The word 'standard' refers to an interface system that does not utilize unused equipment in the other interface system).

4.4.3 Two hybrid computing systems can be mechanized and operated simultaneously and completely independent of one another.

4.4.4 One group of analog computers, one interface system, and one digital computer can be delivered to LMSC where they will be checked out, and operated both independently and as a hybrid computing unit. The remaining computing equipment can be assembled and checked out at another location (e.g. vendor's factory). The interface vendor shall state the change in cost and physical size of the complete interface system if this operational philosophy (4.4.4) is recinded.

4.5 Control

The area of control involves all those functions of the linkage equipment which involve the controllability of the interface system from the digital computer, analog computer, and from the interface logic patch panel. This request indicates what functions must be controlled, but the implementation of these controls is a direct function of the particular analog and digital computers and is left up to the system designer. It will be the responsibility of the vendor to furnish a satisfactory operating system.

This document should be used only to determine the functional capabilities and not be used as a specification for equipment design. The responsibility for linking the equipment to the analog computer and to the digital computer is the responsibility of the vendor. In evaluating the proposed system, Lockheed will be interested in the command structure utilized by the digital computer in controlling the interface. The execution times of these commands will be evaluated and must be contained in the proposal. Every effort should be made by the vendor to implement the functional capability of the equipment with off the shelf design and equipment.

5.0 Data Transmission System:

5.1 General

5.1.1 The transmission and processing of continuous data signals between the analog and digital computers shall be accomplished in each of the two interface systems by the analog-to-digital and the digital-to-analog systems. Analog computer signals shall be digitized and sent to the digital computer via the Analog-to-Digital Conversion (ADC) system (Figure 2). Digital-to-analog signals shall be processed and transmitted to the analog computer via the Digital-to-Analog Conversion (DAC) system (Figure 3).

5.1.2 Control of the ADC sample and hold amplifiers and the DAC output registers shall be governed by the digital computers. However, the system shall be designed such that the two interfaces will have the capability to override and synchronize control by appropriate patching of general purpose logic on the interface patchboards.

5.1.3 A switching arrangement shall be incorporated within the hybrid DAC interface system to provide switching control of unused DAC and/or ADC channels in one interface system to the other interface system.

5.1.4 The discussion and description of the ADC and DAC systems that follow, place a lower limit, not an upper limit, on the characteristics and capabilities of the data transmission system's components. The primary concern of this request is to obtain two independent and flexible sets of ADC and DAC systems that can reliably transmit data between the analog and digital computers at a maximum THROUGH-PUT rate, with a maximum THROUGH-PUT accuracy and resolution, and with a minimum amount of noise and distortion.

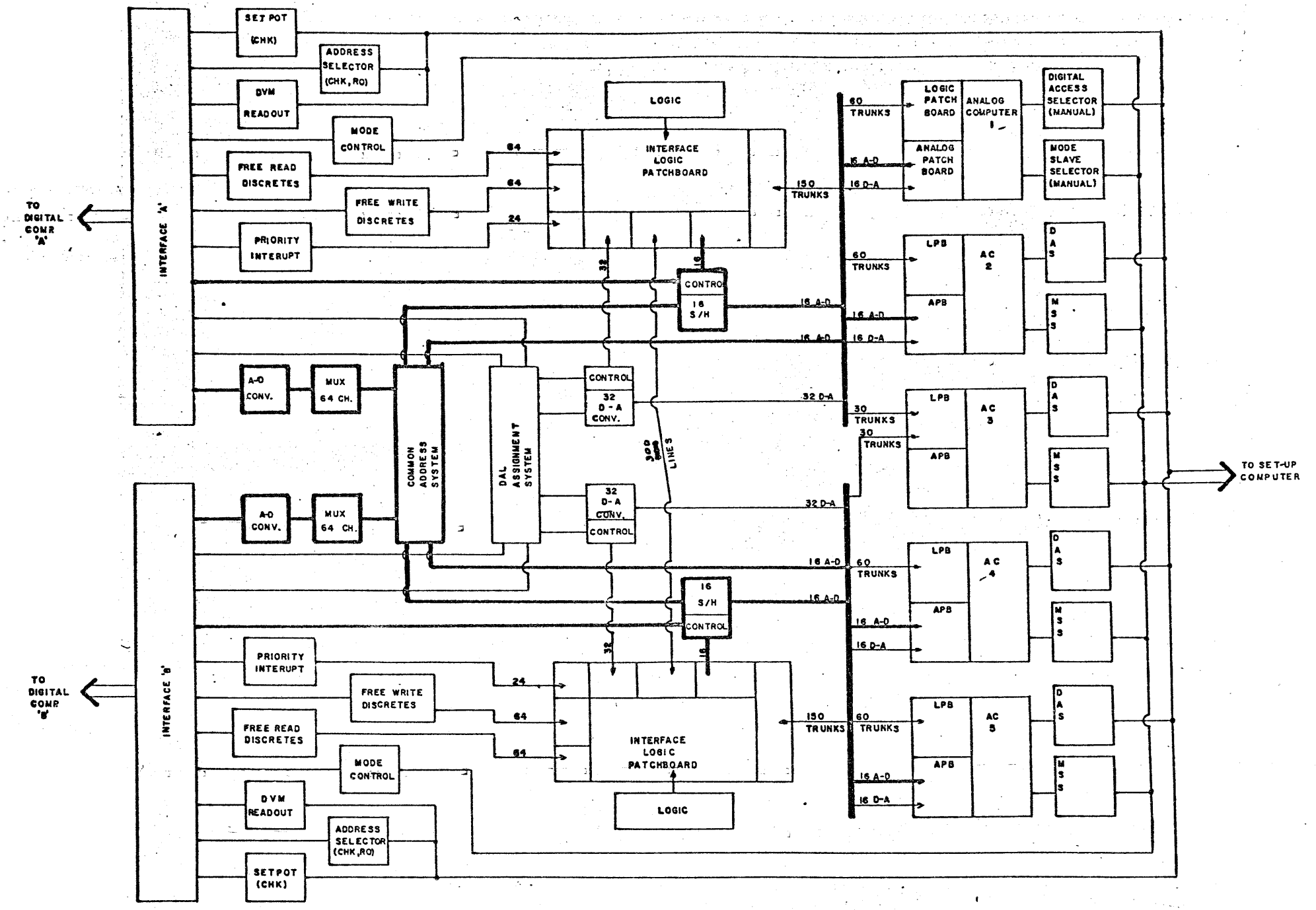


FIGURE 2

ANALOG TO DIGITAL CONVERSION SYSTEM

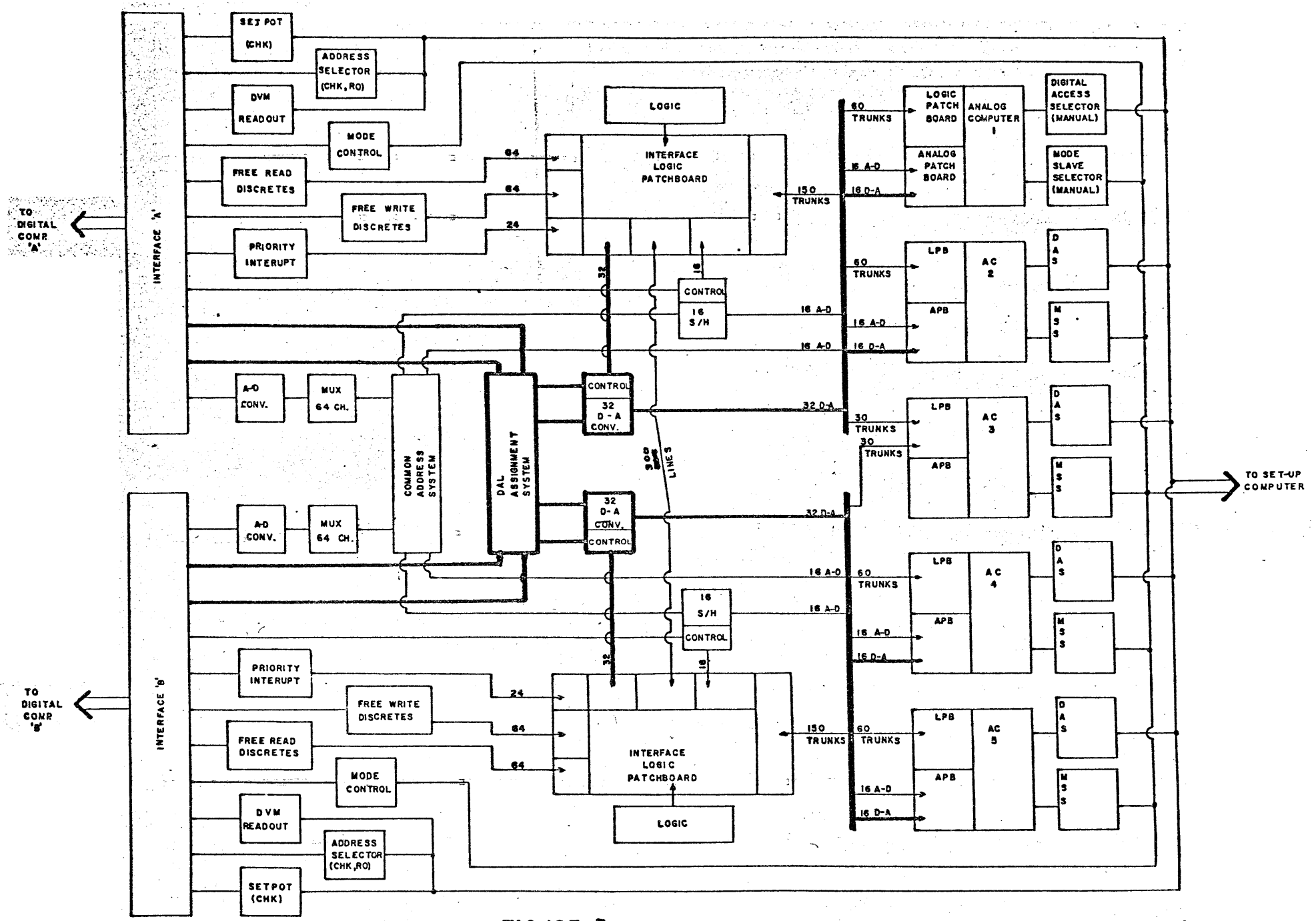


FIGURE 3
DIGITAL TO ANALOG CONVERSION SYSTEM

5.2 ADC Requirements:

5.2.1 General

Each of the two ADC systems (Figure 2) shall include cabinets, chassis, and associated power supplies wired and with all the necessary cabling to the digital and analog computers and:

5.2.2 The hybrid interface shall contain a total of 64 ADC channels -- 32 with sample and hold amplifiers, 32 without sample and hold amplifiers. The vendor is requested to supply a unit or modular price with his proposal for ease of modification.

5.2.3 The ADC channels will be connected to the analog computers' patchboards as shown in Figure 2. Each of the four analog computers (Numbers 1,2,4,5) will be connected to 16 different ADC channels; 8 channels containing sample and hold amplifiers, 8 channels without sample and hold amplifiers.

5.2.4 All ADC channels shall accept analog voltages from the analog patchboards that will range from plus to minus 100 volts. The vendor shall discuss a method by which his proposed ADC system can detect analog input voltages that exceed 100 volts.

5.2.5 All ADC channels will be constructed such as not to degrade the analog computers' operation by excessive loading.

5.2.6 The two ADC systems shall be independent such that a malfunction or power shutdown in one interface system will not affect the standard (See: 4.4.2) operation of the other.

5.2.7 Interface 'A' shall contain the 32 ADC channels connected to analog computers numbered 1 and 2. Interface 'B' shall contain the remaining 32 ADC channels connected to analog computers numbered 4 and 5.

5.2.8 Each interface system shall be able to random and sequentially monitor all ADC channels independently of one another. The vendor should describe the operational modes of his proposed ADC system in detail.

5.2.9 It is desirable that each of the two interfaces contain a multiplexer and address system such that the 64 ADC channels can be expanded up to 96 channels after delivery of the hybrid interface system. The vendor is requested to describe the expansion capability of his proposed ADC systems. He will include two supplementary

prices in his quotation: The price per additional ADC channel with a sample and hold amplifier; the price per additional ADC channel without a sample and hold amplifier.

5.2.10 The ADC resolution shall be 14 bits (13 bits plus sign) or more. If the vendor has the capability of furnishing an ADC system(s) with a resolution exceeding 14 bits, he should document, price and include that system(s) as an option to the 14 bit ADC system. If the vendor has a preference for one ADC system over another (e.g. resolution), he should state his preference within his proposal and discuss his reasons.

5.2.11 The control of the 16 sample and hold amplifiers in each of the two ADC interface systems shall be connected to their corresponding Interface Logic Patchboards (Figure 2) in such a way as to allow signals from the logic patchboards to override and synchronize sample and hold commands originating in the digital computers. The vendor is expected to include a complete description of his proposed sample and hold control system in his proposal. Desirable features of this system would be: If no patching is made to a sample and hold control hole on the logic patchboard, then the sample and hold amplifier represented by that patchboard hole would respond directly to sample and hold commands emanating from the digital computer. A 'disable' signal patched into the hole would delay execution of the digital computers' command until the signal from the logic patchboard changed to 'enable'.

5.2.12 An ADC sample and hold selection switch (manual) shall be included within the hybrid interface system by which an operator could distribute the control of the sample and hold amplifiers between the two digital computers. The switch should functionally operate as follows: If an operator manually positions the switch between numbers n and n+1; Sample and hold amplifiers numbered up to and including n would be under control of digital computer 'A', (digital computer 'B' could monitor the output of the sample and hold amplifiers, but it could not control the amplifiers); sample and hold amplifiers numbered n+1 and greater would be assigned to digital computer 'B' (digital computer 'A' could monitor the output

of the sample and hold amplifiers, but it could not control the amplifiers). Standard ADC system operation would be achieved when the switch was positioned between numbers 16 and 17 (See: 4.4.2)

5.3 ADC System Specifications

5.3.1 General

The manufacturer shall include the following specifications in his description of his proposed ADC system. In these specifications ADC THROUGH-PUT and S/H shall be defined as:

- ADC THROUGH-PUT: From the analog computer's patchboard to the digital computer's memory.
- S/H: Sample and Hold or Track and Store amplifier.

5.3.2 ADC THROUGH-PUT rate 1:

This rate shall specify the speed at which 16 ADC channels with sample and hold amplifiers (S/H) can be sequentially addressed and their voltages digitized and transferred to one of the digital computer's memory storage. The ADC THROUGH-PUT rate shall be commensurate with the THROUGH-PUT accuracy 1. The rate shall be derived under the following conditions:

- S/H amplifiers have previously been placed in their hold (store) mode;
- S/H amplifiers are connected to the first through the sixteenth multiplexer channels;
- The multiplexer shall start with its first channel and advance sequentially to its sixteenth channel;
- S/H amplifiers connected to even numbered multiplexer channels will represent maximum analog output voltages of the opposite polarity as those connected to odd numbered multiplexer channels. (e.g. Chan 1, +100V; Chan 2, -100V; Chan 3, +100V; ...; Chan 16 -100V).

5.3.3 ADC THROUGH-PUT rate 2:

This rate shall specify the speed at which the information on the 17th through the 32nd multiplexer channels (without S/H amplifiers) can be sequentially addressed, digitized and placed in the digital computer's memory storage. The ADC THROUGH-PUT rate shall be commensurate with the THROUGH-PUT accuracy 2. The rate shall be derived under the following conditions:

- The sixteen analog input channels without S/H amplifiers shall be connected to the 17th through the 32nd multiplexer channels;
- The voltages from the analog patchboard on the sixteen direct lines of the multiplexer shall alternate between plus and minus peak analog output voltages (e.g. Chan 17, +100V; Chan 18, -100V; Chan 19, +100V; ...; Chan 32, -100V).

5.3.4 ADC THROUGH-PUT accuracy 1:

This value shall specify the accuracy with which the ADC system can transpose an analog voltage on the analog computer's patchboard (via a S/H amplifier, multiplexer and ADC) into a digitized number and store it within the digital computer's memory. ADC THROUGH-PUT accuracy shall include errors from all contributing sources (e.g. S/H amplifier; ADC resolution; component off-set, gain, linearity; allowable settling times), and shall be that error which is associated with the ADC THROUGH-PUT rate 1. The value shall be specified as a percent of the peak analog output voltage (e.g. $\pm$0.03% of 100 volts).

5.3.5 ADC THROUGH-PUT accuracy 2:

With two exceptions, this specification shall be the same as that described in ADC THROUGH-PUT accuracy 1. Exceptions: The S/H amplifier is not included in the signal line; the error shall be commensurate with ADC THROUGH-PUT rate 2.

5.3.6 S/H Recovery Time:

The length of time necessary for the sample and hold amplifier to change from a state where it is holding (storing) a voltage representing the plus or minus peak analog output voltage to the sample (track) mode where it is accurately tracking the peak analog voltage of the opposite polarity. The accuracy of the track-mode shall be commensurate with the ADC THROUGH-PUT accuracy 1.

5.3.7 S/H Decay:

This characteristic represents the maximum voltage decay (droop) experienced by any of 16 sample and hold amplifiers from the time they were placed into the hold (store) mode to the time the last S/H amplifier was sequentially addressed and its voltage digitized. The initial value of voltage stored on the 16 S/H amplifiers shall correspond to the peak analog output voltage (e.g. 100 volts). The S/H decay shall be specified as a percent of the peak analog output voltage (e.g. 0.005% of 100 volts).

5.4 DAC Requirements:

5.4.1 General

Each of the two DAC systems (Figure 3) shall include cabinets, chassis, and associated power supplies wired and with all the necessary cabling to both the digital and analog computers and:

5.4.2 The hybrid interface shall contain a total of 64 double buffered DAC channels. The vendor is requested to supply a unit or modular price with his proposal for ease of modification.

5.4.3 The DAC channels will be terminated on the analog computers' patchboards as shown in Figure 3. Each of the four analog computers (numbers 1,2,4,5) will be connected to 16 different DAC channels.

5.4.4 All DAC channels shall be referenced to the analog reference voltage supplies of their respective analog computers. The interface must be designed such that the DAC systems do not draw an excessive amount of current from the analog computers' reference supplies.

5.4.5 All DAC channels shall be able to output voltages to the analog computers' patchboards that range from plus to minus 100 volts. The DAC output amplifiers will be expected to drive the same loads as the analog amplifiers. Any significant dissimilarities in electrical characteristics between the DAC output amplifiers and the analog amplifiers shall be noted by the vendor.

5.4.6 The two DAC systems shall be independent such that a malfunction or power shutdown in one interface system will not affect the standard (See 4.4.2) operation of the other.

5.4.7 Interface 'A' shall contain the 32 DAC channels connected to analog computers numbered 1 and 2. Interface 'B' shall contain the 32 DAC channels connected to analog computers numbered 4 and 5.

5.4.8 It is desirable that each of the two DAC systems have the capability of expanding in number of channels after delivery of the hybrid interface system. The vendor is requested to describe the expansion capability of his proposed system. He should include the unit or modular price required for this expansion.

5.4.9 The DAC resolution shall be 14 bits (13 bits plus sign) or more. If the vendor has the capability of furnishing an DAC system(s) with a resolution exceeding 14 bits, he shall document, price and include that system(s) as an option to his 14 bit DAC system.

If the vendor has a preference for one DAC system over another (e.g. resolution, buffers) he should state his preference within his proposal and discuss the reasons for his preference.

5.4.10 The control of the 32 output registers in each of the two DAC interface systems shall be connected to their corresponding interface logic patchboards in such a way as to allow signals from the logic interface patchboards to override and synchronize output register transfer commands originating in the digital computers. The vendor is expected to include a complete description of his proposed output register control system within his proposal. Desirable features of this system would be: If no patching is made to an output register control hole on the logic interface patchboard, then the output register represented by that patchboard hole would respond directly to output register transfer commands emanating from the digital computer. A 'disable' signal patched into the hole would delay execution of the transfer command until the signal changed to 'enable'.

5.4.11 A DAC assignment switch (manual) shall be included within the hybrid interface system which will enable an operator to assign the DAC channels associated with each of the two digital computers. The position of this switch will determine which of the two digital computers can send input data into a DAC's input register and send control commands to the DAC's output register. The vendor is expected to include a complete description of this control system in his proposal. The switch should have the following characteristics: If an operator manually positions the DAC assignment switch between numbers n and n+1; DAC channels numbered up to and including n would be assigned to digital computer 'A' (digital computer 'B' could neither send data nor control commands); DAC channels numbered n+1 and greater would be assigned to digital computer 'B' (digital computer 'A' could neither send data nor control commands). Standard operation would be achieved when the switch was positioned between numbers 32 and 33 (See: 4.4.2).

5.5 DAC System Specifications:

5.5.1 General

The manufacturer shall include the following specifications in his

description of his proposed DAC system. In these specifications, DAC THROUGH-PUT shall be defined as:

- DAC THROUGH-PUT: From digital computer memory storage to analog computer patchboard.

5.5.2 DAC Amplifier settling time 1:
Length of time necessary for one DAC output amplifier to change from a plus or minus peak analog output voltage to a peak output voltage of the opposite polarity (e.g. from -100V to +100V). The settling time shall be sufficient to provide the DAC THROUGH-PUT accuracy.

5.5.3 DAC Amplifier settling time 2:
Length of time necessary for one DAC output amplifier to change from a plus or minus peak analog output voltage to 99% of the peak voltage of the same polarity (e.g. from -100V to -99V). The settling time shall be sufficient to provide the DAC THROUGH-PUT accuracy.

5.5.4 DAC THROUGH-PUT signal-to-noise ratio:
This figure shall represent the ratio of the noise amplitude on the DAC channel measured at the analog patchboard to the peak analog output voltage (e.g. $\pm$0.005% of 100 volts).

5.5.5 DAC THROUGH-PUT accuracy:
This value shall include errors from all contributing sources (e.g. DAC resolution; component off-set, gain error, linearity error; allowed settling time) and shall be that error associated with the specified DAC THROUGH-PUT rates. The value shall be specified as a percent of the peak output voltage (e.g. $\pm$0.01% of 100 volts).

5.5.6 DAC THROUGH-PUT rate 1:
The length of time required to change 32 DAC channels assigned to one digital computer from a plus or minus peak analog voltage output to a peak amplitude output of the opposite polarity. The length of time shall include the time necessary to sequentially load the DAC input registers from the digital memory, the updating of the output registers in unison, and the DAC output amplifiers' settling time. The allowed settling time shall be commensurate with that used in deriving the DAC THROUGH-PUT accuracy.

5.5.7 DAC THROUGH-PUT rate 2:

With one exception, this specification is the same as the procedure for DAC THROUGH-PUT rate 1. Exception, the DAC output voltage to the analog patchboard shall retain the same polarity and be commanded to change from 100% to 99% of a peak value (e.g. +100V to +99V).

5.6 Isolation:

The vendor shall describe and evaluate the effectiveness of the techniques he will utilize to minimize noise and distortion in his proposed data transmission system (e.g. analog-interface-digital ground loops, cross talk).

5.7 Checkout Panel:

It would be desirable if the vendor's interface system contained a checkout panel by which the interface and analog computer sections of a hybrid simulation could be statically checked and trouble shot without the use of the digital computers. If available and practical, the vendor should include in his proposal a description of the control panel's functions for evaluation and consideration. The checkout panel should provide for:

- Digital values to be loaded into the DAC registers.
- Digital values to be read out of the ADC registers.

5.8 Optional Configuration:

More than one data transmission system configuration may be acceptable since there are trade-offs between the data transmission system's characteristics (i.e., settling time versus rate versus accuracy versus resolution). If a trade-off enhances one or more ADC or DAC system characteristic (e.g., greater THROUGH-PUT accuracy, rate, resolution), without violating the minimum requirements, the vendor should note the option and document the associated specifications.

6.0 General Purpose Logic:

General purpose logic will be added to the hybrid interface system to supplement the logic contained on the analog computers' logic patchboards (Figure 4). This logic with its associated patchboards will be supplied with the hybrid computer interface. Logic will be divided into two groups each associated with one of the two digital computers. The logic power supplies, cables and associated components will be made as independent as possible so that a malfunction or a

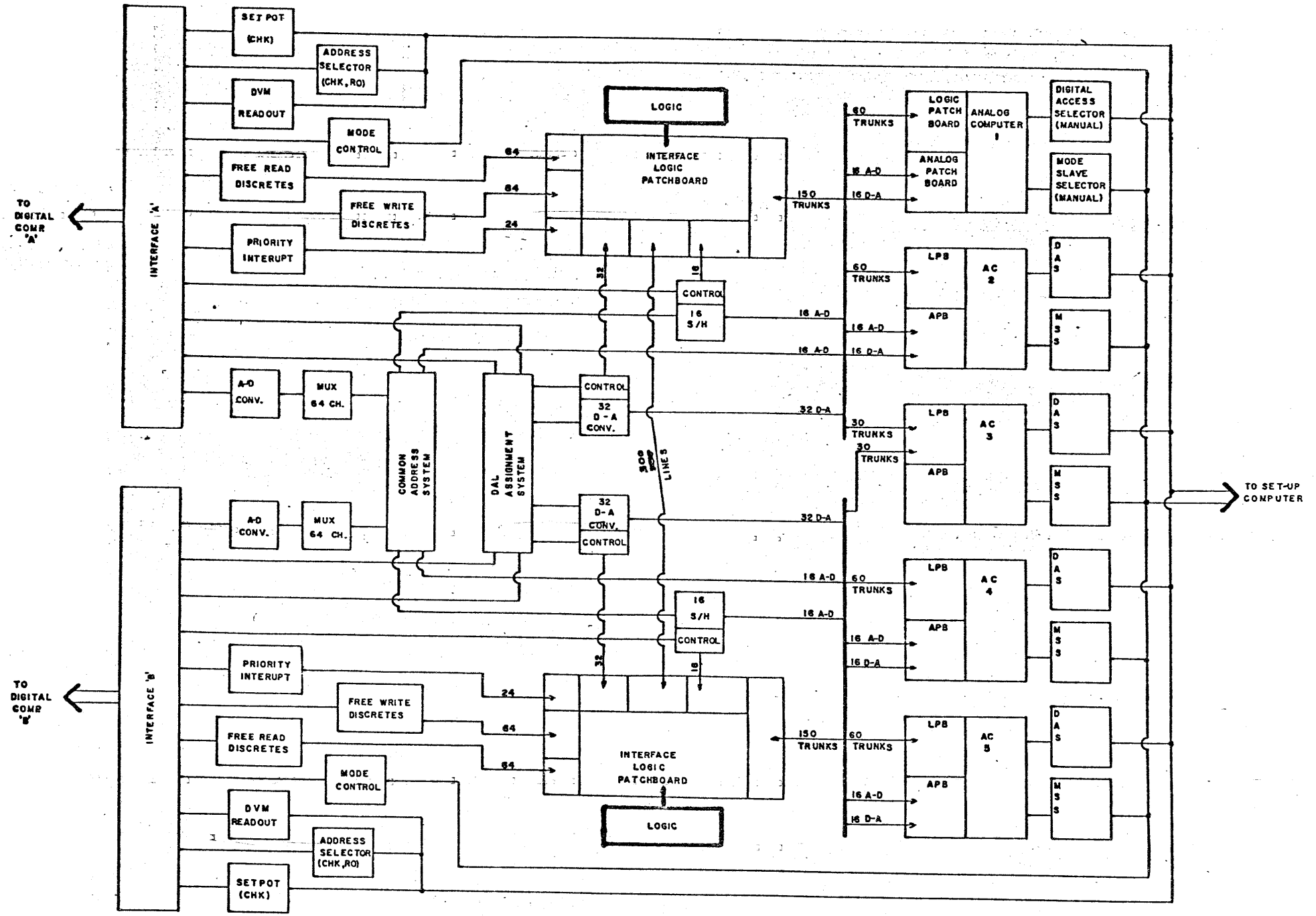


FIGURE 4
GENERAL PURPOSE INTERFACE LOGIC

power shutdown on one of the logic complements will not interfer with the operation of the other.

6.1 Logic Complement:

Each of the two interface systems will contain 2 patchboards, an assortment of patch leads and the following logic complement:

1 clock (1-2 MC)

36 decode down counters

80 flip flops

10 one shots

10 differentiators

200 two-input 'AND' gates

50 five-input 'AND' gates

10 line drivers

All logic outputs will have the capability of driving at least 8 other logic units. The logic complement should be optionally priced so that the complement can be easily modified.

6.2 Patchboard Terminations:

Each interface patchboard will contain the discrete and interrupt information from its associated digital computer, the outputs and inputs from its associated general purpose interface logic, trunk lines between the two logic interface patchpanels and discrete trunk lines to three of the analog computers (figure 5). The complements of logic signals should be available and as much bussing as possible as determined by the interface patchboard size selected by the vendor. Both interface patchbays should be designed identically so that patchboards wired for interface 'A' can be run on interface 'B'.

6.3 Logic Compatibility:

6.3.1 The trunks between the interface logic patchboards and the interface logic shall be designed so that logic from one logic complement can be patched and used as part of the other logic complement (Figure 5).

6.3.2 The logic on the interface patchboards should be compatible with the logic on the analog computers' logic patchboard. If it is not compatible, then signal conditioning for a 150 bi-directional signal (level changers) will be provided on each of the two interface patchboards. If bi-directional signal conditioning is

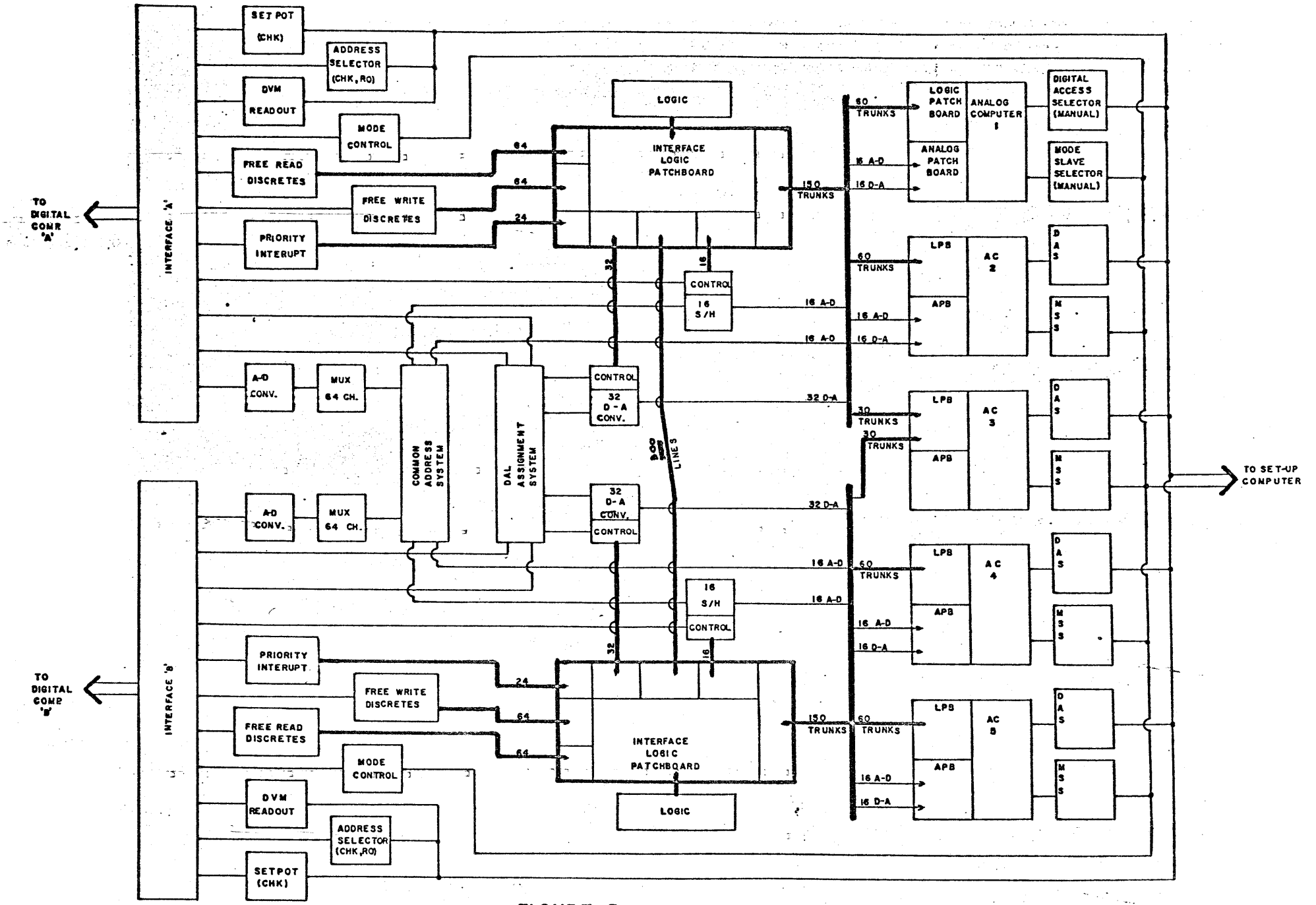


FIGURE 5
INTERFACE PATCHBOARD TERMINATIONS

not a practical approach, then a 100 input and a 100 output signal conditioning unit (level changers) shall be supplied for each of the two interface systems.

6.3.3 All computer discretes will be terminated on their respective interface logic patchboards. This will include control lines (9.0) status lines (9.0), and interrupt lines (8.0). These lines will originate at the interface of the digital computer and shall be compatible with the logic levels of the general purpose interface logic.

6.4 Synchronous Logic:

The vendor will discuss the problems of synchronous and asynchronous patchable logic. He will discuss how logic and clock information will be synchronized between analog computers and the interface systems between slaved analog computers, between interfaces, between combinations of each, especially when independent problems share the same logic patchboards. The vendor should state his ability to provide both synchronous and asynchronous logic. He should include within his quotation the prices for both types of logic.

7.0 Discrete Trunks:

7.1 General:

Interface systems 'A' and 'B' shall be able to transmit discrete signals from one interface logic patchboard to another and to the analog logic patchboards through a system of general purpose discrete-trunk lines (Figure 6). The trunk lines shall be arranged and/or constructed such that crosstalk does not degrade the overall hybrid system's performance.

7.2 Analog-Interface Trunks:

Each interface system shall have 150 general purpose discrete-trunk lines which will be connected from its interface logic patchboard to three of the five analog computers. Interface 'A' will have 60 of its 150 lines connected to the analog logic patchboard of analog computer number 1, 60 lines connected to analog computer 2, and 30 lines connected to analog computer 3. Interface 'B' will have 60 of its 150 discrete-trunk lines connected to the logic patchboard of analog computer number 5, 60 lines connected to analog computer 4, and 30 lines connected to analog computer 3. All lines shall terminate in well defined patchboard locations and in such a way that all analog logic patchboards are similar and interchangeable.

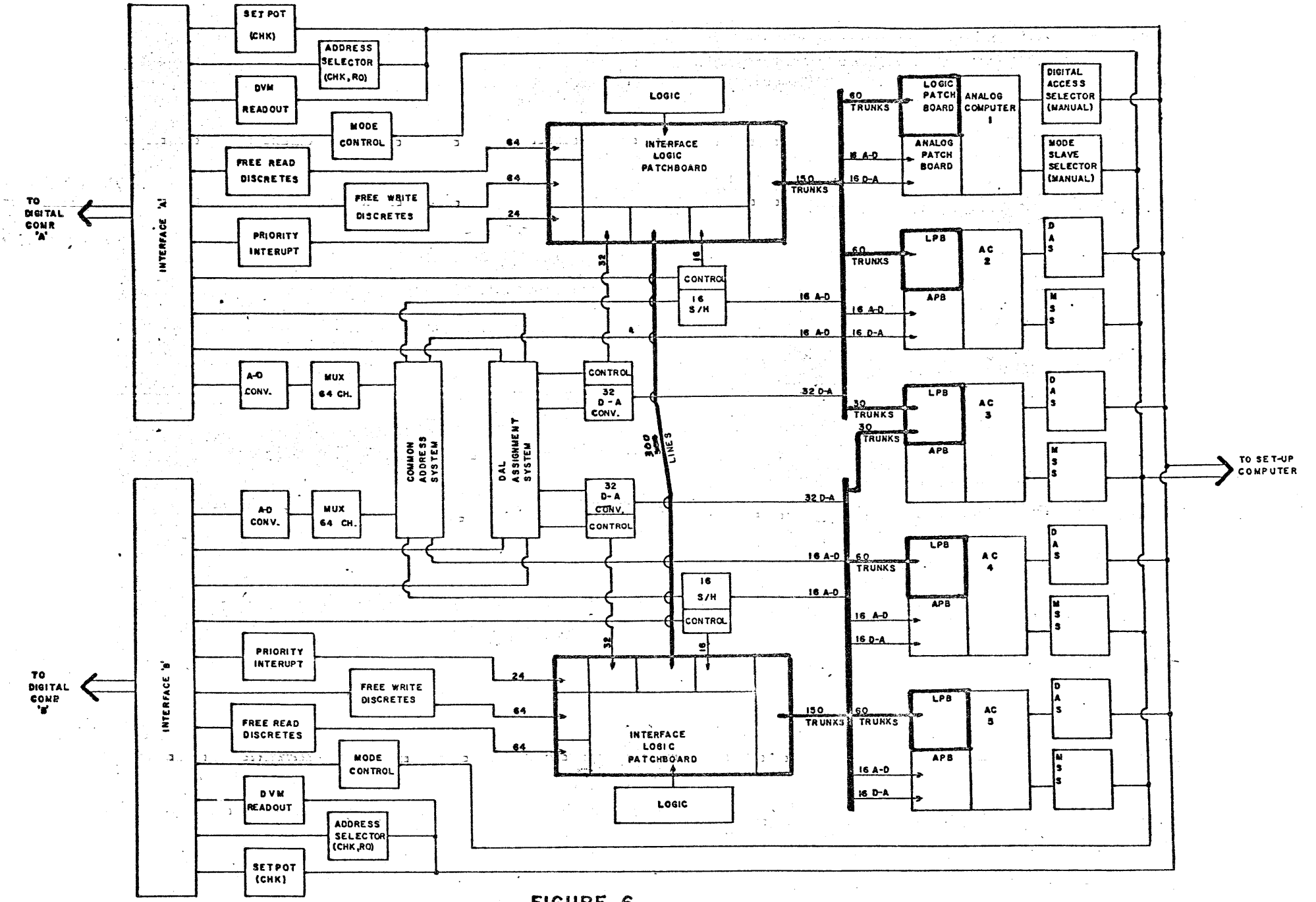


FIGURE 6

DISCRETE TRUNKS

Interface logic patchboards shall be similar and interchangeable with one another. The vendor shall submit a modular or unit price for these lines with his regular quotation to facilitate ease of modification.

7.3 Interface-Interface Trunks:

The two interface logic patchboards will be connected to one another by 300 general purpose discrete lines (Figure 6). These lines will be terminated in well defined locations on each of the two interface's patchboards such that their patchboards are interchangeable. The vendor shall include a modular or unit price for these lines with his regular quotation for ease of modification.

8.0 Free Priority Interrupts:

8.1 General:

The interrupt portion of the interface equipment is of vital importance in evaluating the vendor's proposal. It is the responsibility of the interface vendor to insure that this hybrid computer system has two independent priority interrupt systems - one for each digital computer (Figure 7). Due to the vital nature of this system, complete specifications of the command functions and the operational registers must accompany the proposal for evaluation. Both 'A' and 'B' interfaces will have 24 non-assigned (free) interrupts that are connected on their respective logic interface patchboards. The interrupt logic levels shall be compatible with the logic levels of the general purpose interface logic.

8.2 Description:

The operation of the interrupt system will depend greatly on the digital computer selected for the hybrid computing system. The interrupt characteristics desired in this proposal are described as if the interrupt capability had to be designed within the interface system. The following interrupt scheme is a suggested method of handling interrupts. The interrupt control of the interface system will be used by the digital computer to allow interrupts of higher priority to be processed while disallowing interrupts of lower priority. This system will be effected by an interrupt register and an interrupt mask register. The interrupt mask register will allow a bit set in the interrupt register to be transmitted to the digital computer on its associated interrupt line. If the bit is zero in the mask register, transmission will be disallowed. The interrupt register will be set by a signal from the analog computer and is reset by the digital computer.

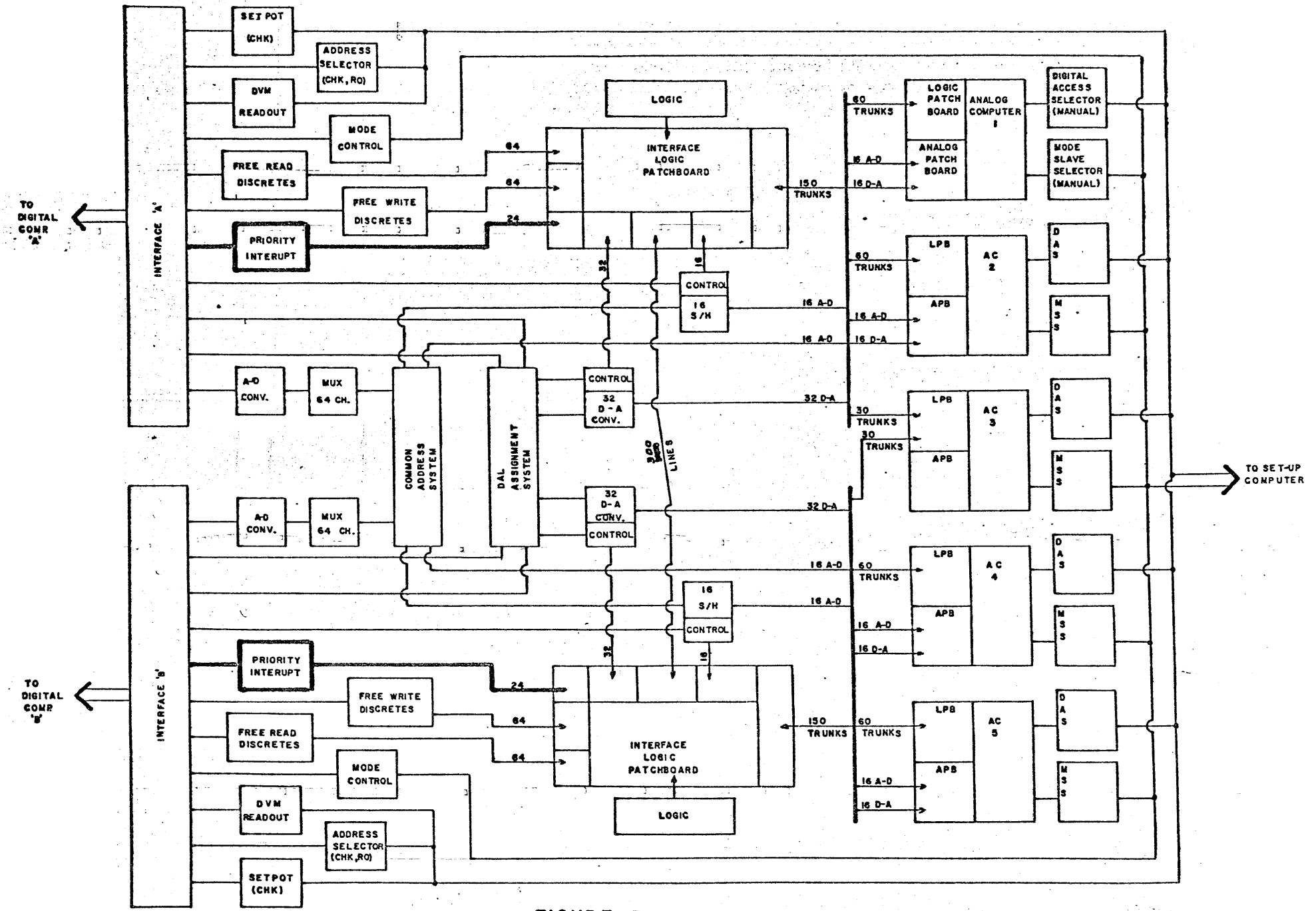


FIGURE 7
FREE PRIORITY INTERUPT SYSTEM

The digital computer may reset the interrupt register or each bit selectively. The interrupt register will continue to drive its associated interrupts through the mask register until reset by the digital computer even if the controlling signal from the analog computer or interface logic disappears.

9.0 Free Discretes:

9.1 General:

The two interface systems will each contain 64 read and 64 write discrete lines (Figure 8). The lines will be terminated in well defined locations on the interface patchboards in such a way as to allow the interface patchboards to be interchanged. These read and write sense and control lines will be able to be sensed and selected by the digital computer. The manner in which these discrete lines are implemented will be determined by the selection of the digital computer. If the digital computer has the capability of selecting control lines and of sensing individual discrete lines then the interface will merely contain the logic required for signal conditioning these signals for the interface patchboard in the flipflops required for storage of these lines. If a digital computer is selected without this capability, then the interface must contain the decoding of channel commands required to implement the selection and sensing of control lines.

9.2 Parallel and Individual Control:

A desirable feature would be the division of the read-write discrete lines into two groups - one which would be controlled by parallel transfer and the other which would allow individual sensing and select. The parallel transfer would appear on the interface patchboard as a input and a output register. The individual lines would appear on the patchboard as simple control and discrete lines.

9.3 One Shots:

A desirable feature for the control lines would be the ability for patching automatic reset. In this mode of operation, by placing the plug in the interface patchboard, the flipflops storing the control line would be reset generating a pulse signal at the interface patchboard. The pulse should be at the length and levels required for satisfactory operation with the logic on the interface patch panel.

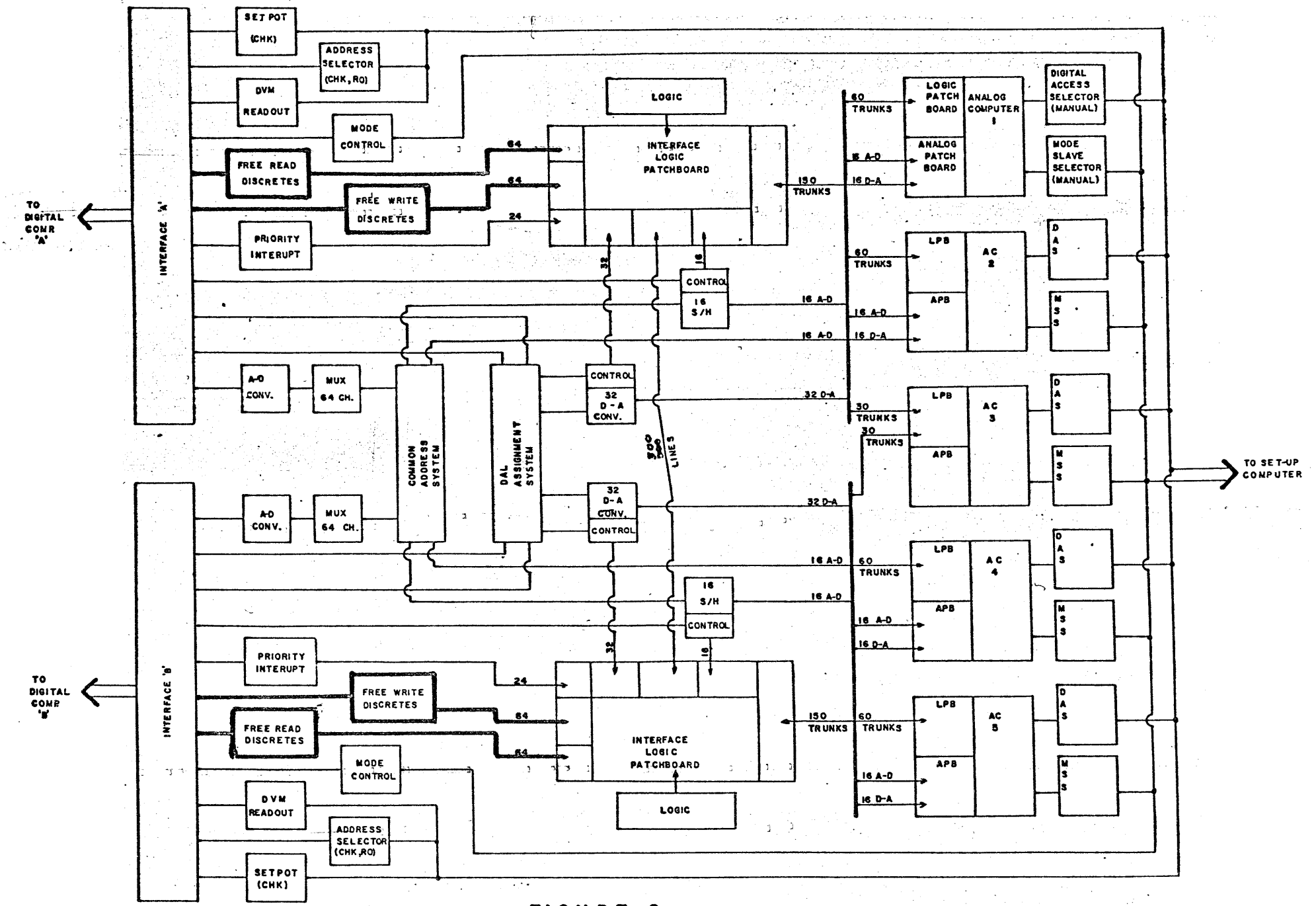


FIGURE 8

FREE READ & WRITE DISCRETE SYSTEMS

10.0 Functional Control:

10.1 General:

The control section of the interface will allow the digital computer to perform set-up, control, and monitoring functions within the analog computer. These functions are:

- DVM Readout (Figure 9)
- Set Pot (Figure 9)
- Address Select (Figure 9)
- Mode Control (Figure 10)

A dual channel controller from the digital computers with access up to five analog consoles will be furnished. Both digital computers will be able to operate in parallel with any of the analog consoles.

10.2 Digital Access Selection:

A digital access selector switch will be installed on each analog computer (Figure 9). This switch will allow communication from digital Computer 'A' only; allow access from digital computer 'B' only; allow access from both digital computers; or allow access from neither digital computer. An additional switch position will allow complete isolation of the analog computer from the interface controller and allow direct access by a small digital set-up computer.

10.3 Addressing an Analog Computer:

The digital computer will be able to address an analog computer by sending an address selection code to the interface controller. When the address for the analog computer is received, the interface will determine whether the digital access selection switch is in the proper position to allow access by that digital computer. A check will also be made to see if the analog computer is currently reserved by the other digital control interface. If the analog computer is not reserved and the digital address selection is allowed, the analog computer will be reserved by the addressing computer until a release command is sent by the digital computer. Any attempts to address the analog computer by the other digital computer will be rejected until this release command is sent. However, the other digital computer may communicate with any of the other analog computers whose digital access selection switch allows its addressing. If the controller rejects a digital computer, status information will be furnished so that the digital computer may determine the reason for the rejection.

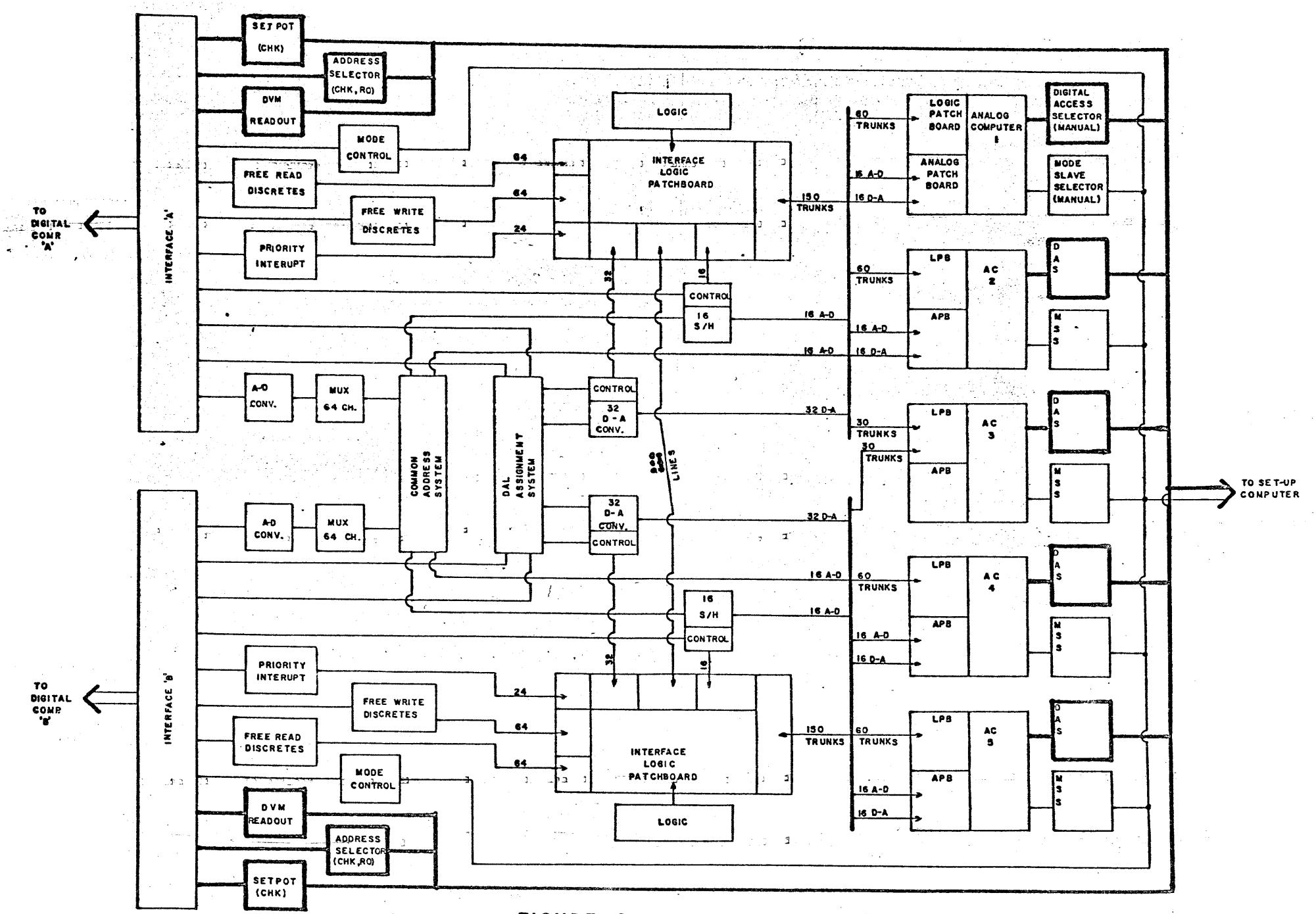


FIGURE 9

ADDRESS SELECTOR, DVM READOUT & SETPOT SYSTEMS

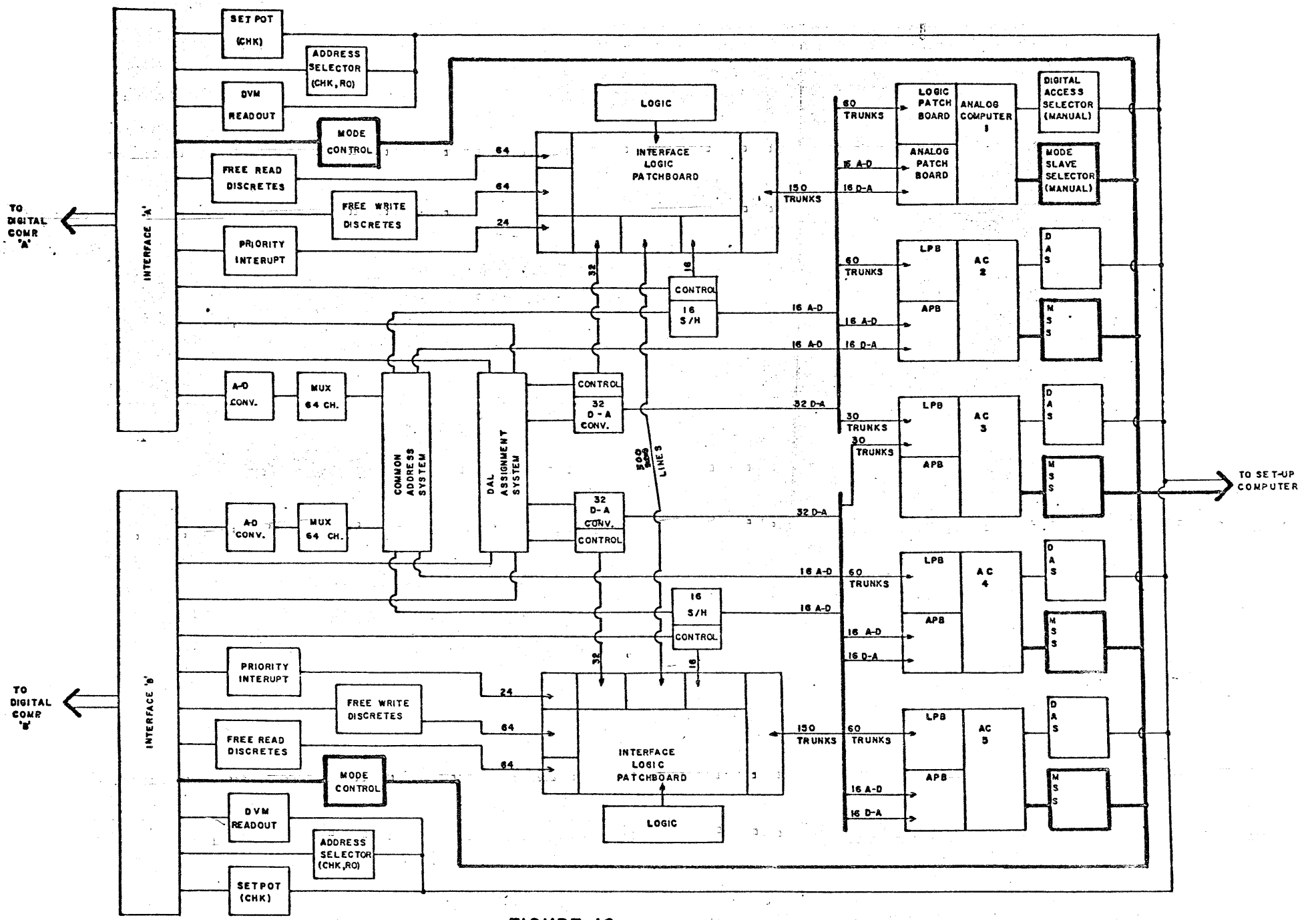


FIGURE 10
MODE CONTROL SYSTEM

10.4 Busy Status and End of Operation Interrupt:

If the operation selected by the digital computer cannot take place within the speed required for the digital computer to execute a further command, this function will cause the activation of a busy sense line. This busy sense line will stay set until the operation is completed. The hybrid computer programmer will also have the option of selecting an interrupt on end of operation. This interrupt will allow the digital processor to continue on other calculations and be interrupted when the slower function requested of the analog computer is completed. All functions on the analog computer of which the controller cannot complete at computer speed, will utilize this busy and interrupt on end of operation signals.

10.5 Address Selection:

The digital computer, through the controller, will be able to select any computing component on the analog computer's patchboard that can be selected by the analog computer's address selection system (Figure 9).

10.6 DVM Readout:

The computer may readout any analog component of the analog patchboard which has been previously selected by an address select command (Figure 9). The DVM readout may be selected with or without an interrupt on the end of the operation.

10.7 Setting Pots:

The digital computer may set a pot on the analog computer whose address has been previously selected (Figure 9). This action will incorporate a command to place the pot in the check submode. The operation may take place with or without interrupt on the end of operation. The controller will raise the busy status line as long as the operation is taking place. Before dropping the status line or generating an interrupt to end of operation, a error set pot status bit will be set if the pot could not be set within the required tolerance.

10.8 Mode Control:

The interface will be able to slave to the mode of a master analog computer or the analog computers will be able to slave to the interface. Status information as to the mode of the master analog computer or the interface will be available to the digital computers. The digital computer will be able to control all the modes of the analog computer when the analog

computers are slaved to the interface (e.g. run, hold, initial condition, pot set, rate test, status test). The selection of the slaving of each analog computer will be under control of a manual mode slave selector switch located on each of the five analog computers (Figure 10). The functions of this switch are a supplement to the analog computer's own mode slaving system.

11.0 Cabling:

11.1 General:

The interface vendor shall assume responsibility for the construction and installation of all cables (e.g. control, power and data transmission), necessary to integrate each of the two interface systems into the desired hybrid computing system.

11.2 ADC Channels:

16 ADC channels from interface 'A' (8 with, 8 without S/H amplifiers) shall be cabled to analog computer 1 (Figure 2). The remaining channels will be cabled to analog computer 2. These channels will be terminated in a well defined location on the analog logic patchboards. ADC channels from interface 'B' shall be cabled and terminated to analog computers 4 and 5 in the same fashion.

11.3 DAC Channels:

16 DAC channels from interface 'A' shall be cabled to analog computer 1 (Figure 3). The remaining 16 channels will be cabled to analog computer 2. These channels will terminate in a well defined patchboard location. The DAC channels from interface 'B' shall be cabled and terminated to analog computers number 4 and 5 in the same fashion.

11.4 Discrete Trunks:

60 trunk lines from interface logic patchboard 'A' shall be cabled to (Figure 6) analog computer 1, 60 to analog computer 2, and 30 to analog computer 3 (Figure 6). These lines will be terminated in a well defined location on the analog logic patchboards.

The trunk lines from interface logic patchboard 'B' shall be cabled and terminated to analog computers 3, 4 and 5 in the same fashion: 60 trunks to analog computer 5, 60 trunks to analog computer 4, and 30 trunks to analog computer 3.

12.0 Installation Requirements:

The hybrid computer installation will be on a false floor with ducted air

conditioning to the computers equipment cabinets. Three phase 115 volt, 60 cycle power is available. The vendor will furnish installation information for all equipments and including:

- Any unique equipment or requirements
- Floor loading
- Power Requirements
- Suggested Layouts
- Layout Restrictions
- Air conditioning and environmental requirements
- Maintenance and space requirements
- Dimensions and floor cutouts for each cabinet
- Maximum and desired cable lengths.

13.0 Documentation Requirements:

The vendor shall deliver to LMSC two complete sets of interface documents at the same time he delivers the interface. Each set shall contain complete and accurate manuals on: Wiring and installation schematics; maintenance and operational procedures.

14.0 Software Requirements:

Software will be required to satisfactorily demonstrate the effective operation of the interface system. The vendor is referred to the software requirements outlined in the digital section of the RFP entitled "LMSC Hybrid Computer, Digital Section". Effective interface diagnostic and maintenance routines will be evaluated as part of the system's total capability and are a very desirable feature. A proposal by the vendor whereby the acceptance software would encompass sophisticated interface, diagnostics and maintenance routines, would be given due consideration by Lockheed.

LOCKHEED MISSILES AND SPACE COMPANY

HYBRID COMPUTER

DIGITAL SECTION

INDEX

1.0 Title:

Lockheed Missiles and Space Company, Hybrid Computer Digital Section.

2.0 Purpose:

The purpose of this RFP is to set forth the requirements of the Digital Section of the Hybrid Computational Facility for Lockheed Missiles and Space Company, Sunnyvale, California. This section of the proposal will deal with the digital computer and its peripheral equipment. This section will also contain the software which is required for the hybrid facility.

3.0 Introduction:

The Hybrid Computer Laboratory will contain two medium sized digital computers and a number of analog consoles. The equipment is expected to solve hybrid, pure digital, and pure analog problems.

The computer system is described in Figure D-1. The system may be divided and operated as two independent systems, or combined to form one large computational system. In the early stages of system operation, the system will operate in a number of fixed configurations. As system capability is increased, the system will become an integrated computational system where equipment allocation is under program control.

The Digital Section of this proposal involves furnishing the digital computer and associated digital peripheral equipment which will be integrated into an operational hybrid system. The requirements of this system have been evaluated and are presented.

Alternate implementations of this capability will be evaluated, if presented, if they are within the framework of the operational philosophy and fulfill the system requirements.

4.0 Digital Computer Hardware:

4.1 Processors

The computer's main frame will consist of two medium speed computers. Alternate configurations of a large processor may be presented. These computers will be evaluated according to their capability of performing high speed scientific computations and their ability to be systemized in a hybrid environment. A secondary consideration of importance will be the effectiveness of their operation as a time shared system.

4.1.1 Hardware Floating Point

The system will be required to have hardware floating point with an accuracy of at least ten decimal digits. The computer will be

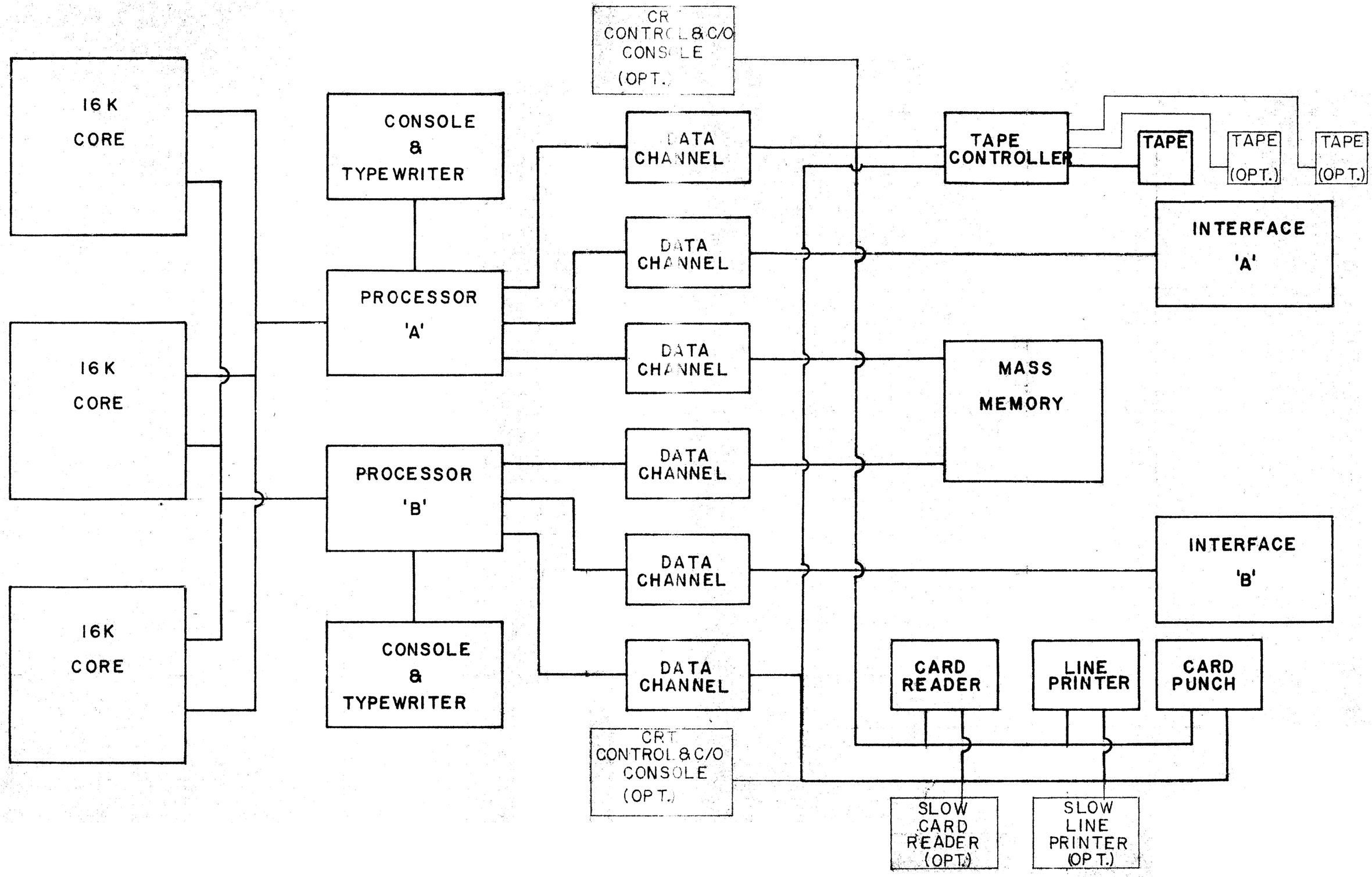

16K CORE
16K CORE
16K CORE
CONSOLE & TYPEWRITER
PROCESSOR 'A'
PROCESSOR 'B'
CONSOLE & TYPEWRITER
CR CONTROL & C/O CONSOLE (OPT.)
DATA CHANNEL
DATA CHANNEL
DATA CHANNEL
DATA CHANNEL
DATA CHANNEL
CRT CONTROL & C/O CONSOLE (OPT.)
TAPE CONTROLLER
TAPE
TAPE (OPT.)
TAPE (OPT.)
INTERFACE 'A'
INTERFACE 'B'
MASS MEMORY
CARD READER
LINE PRINTER
CARD PUNCH
SLOW CARD READER (OPT.)
SLOW LINE PRINTER (OPT.)

FIGURE 2-1

evaluated on its speed in operating on floating point numbers with the following minimum requirements: floating add, 20 microseconds, floating subtract 20 microseconds, floating multiply, 30 microseconds, and floating divide, 30 microseconds. The speed of the floating point arithmetic unit will be evaluated by the instruction timing, execution time of standard arithmetic routines, and execution time of a Fortran compiled program.

4.1.2 Interrupts

Each compute module must contain a multi-level interrupt system. This system will contain the interrupts required for controlling the standard peripherals plus 24 free interrupts for the analog computer interface. Interrupts will be supplied with the ability to arm or disarm each selectively under program control. The vendor will comment on each of the following subjects:

1. Interrupt expansion
2. $I_n$terrupt priorities
3. The effect of shared core on the interrupt system.

4.1.3 Control and Status Lines

The digital computer will be evaluated on its ability to directly control external status and control lines. Optional pricing should be included for such lines as may be required for the vendor furnishing the computer interface.

4.1.4 Core Addressing

The manufacturer will discuss the method by which each processor is addressing the 48K of memory specified in Section 4.2. If the memory addressing scheme is non-standard, a complete documentation is required of the effect of this non-standard memory addressing on the vendor's software.

4.1.5 Time Sharing Hardware

The ability of the computer to be utilized as a time shared system will be discussed. Hardware features such as memory protection and dynamic relocation will be discussed.

4.1.6 Internal Clock:

Each processor will contain an internal clock.

4.2 Memory Requirements

The memory requirements of the digital system are 48K of 24 bit memory or its equivalent. The memory cycle time will be two microseconds or less.

The memory size was calculated on the basis that, (one) computer instructions are stored per memory word, and (two), storage cells are required for floating point numbers. The floating point numbers will be of the accuracy required for ten decimal digits. The maximum memory module size is 16K with each processor having independent access.

4.3 Data Channels

Each compute module will contain a data channel for the standard peripherals, and a data channel for the mass memory. Additional data channels will be required for the analog interface as determined by its vendor. The vendor shall indicate the variety of standard data channels available for interfacing.

4.4 Peripherals

The digital computer peripherals will be specified in this section. The peripheral speeds are indicated as a minimum requirement.

4.4.1 Card Reader

The system will contain a card reader which is accessible to either computer. This card reader will have the capability of reading a standard IBM card at the rate of at least 800 cards per minute. Optional pricing will also be included in the proposal for a high speed card reader on Computer A, and a low speed card reader on Computer B.

4.4.2 Printers

The system will contain a high speed printer capable of printing 1000 lines per minute. Optional pricing will be included for a high speed printer on Computer A, and a low speed printer on Computer B. The printer will have a minimum of 120 print positions per line.

4.4.3 Tape Units

If the vendor does supply a large scale mass memory and has disc oriented software, only one tape unit is required. However, if the vendor does not supply disc oriented software, then a number of tape units will be determined as required to perform effectively the vendor's furnished software system for two computer systems. The tape units will be 1/2 inch IBM compatible tapes with selectable densities of 200, 556 and 800 bits per inch and a speed of at least 75 inches per second.

4.4.4 Punch

A 100 card per minute punch which has the capability of punching both BCD and Binary cards will be required in the system. It would be desirable that this punch could be addressed by either computer, however, if unfavorable cost considerations occur, the punch should be placed on Computer A.

4.4.5 System Control and Checkout Consoles

Two charactron tube consoles with input capability will be included as options in the proposal. These consoles would be utilized for hybrid and digital program modification.

4.4.6 Optional Capability

The vendor should present in this section any hardware capability he has which would provide effective tools for this system.

4.5 Mass Memory

The system will contain a large scale disc storage device which can be accessed by either computer. The size of this disc should be determined as follows: If the vendor is proposing a system which would operate under the basic configuration, and is not disc oriented in operation, then the mass memory storage are two million computer words plus storage for the complete system library. If the vendor is proposing a time sharing system as described under the Time Sharing Operating Philosophy, then a mass memory of 10 million words plus is required. The utilization of mass memory will be determined on how well the vendor's system is oriented to operation with a disc and how well the vendor's system can process in a time sharing mode.

4.6 Interface

4.6.1 Vendor's Ability

The proposal will contain a statement by the vendor of his willingness to supply the interface between the digital and the analog computers. A discussion of the vendor's capability in providing interface systems will be discussed.

4.6.2 System Responsibility

If the vendor is selected as the provider of the digital system, he may be asked to extend his contract to include complete system responsibility. The vendor should make a clear statement of his willingness to take this responsibility and state any reservations.

4.7 Installation Requirements

Computer installation will be on a false floor with ducted air conditioning

to equipment cabinets. Sixty cycle voltages are available. The vendor will furnish complete installation information for all equipment. Including:

1. Any unique equipment or requirements
2. Floor loading
3. Power requirements
4. Suggested layouts
5. Layout restrictions
6. Air conditioning and environmental requirements
7. Maintenance and space requirements
8. Dimensions and floor cutouts for each cabinet.

5.0 Software - Introduction

The software section of this proposal will be discussed under a number of subject headings. Vendors may or may not wish to respond to certain sections of the software required. Exceptions should be made by the vendor for each section of software for which he does not wish to supply. Other software sections may be bid as optional capability. The vendor should, for each software category, clearly indicate in his proposal whether:

- The software outlined in that section is part of his present operating system
- Whether he intends to develop this software capability
- Whether he desired to develop the software required at additional cost
- Whether he desires to take exception to this software capability.

Some software capabilities requested may not be desirable in machine configurations proposed. For example, if a vendor proposes a hardware system which does not have effective time sharing capability, then the section requesting time sharing software should be responded to in that effect. Any software which is to be provided by the vendor will be sufficiently documented so that the capability of such software may be evaluated. This may be done by a description of the software in the proposal, or by including with the proposal the appropriate reference documents. Any software which will be developed by the vendor for this system must include a schedule of completion. If the software to be developed will not be completed within a safe schedule of the delivery of the system, a complete description of the basic operating capability for hybrid and digital computation must be provided.

5.1 Requirements

The hybrid simulation laboratory must be able to handle the following type jobs: Two hybrid simulations, one large hybrid simulation, all digital scientific computation, and all analog simulation problems.

5.1.1 Hybrid Requirements

There are certain requirements needed for effective hybrid computation in the programming system. The hybrid programmer is effectively simulating a system under design. He is using the analog computer to allow him to use flexibility in system design and parameter modification. This same type of hands on features must be carried into the digital program. This statement implies many far reaching possibilities in the effectiveness of the hybrid programmer to modify his program and parameters while operating at the console. It will not be the purpose of this RFP to state in what way the vendor will propose to effectively give the operator this capability. Such methods may include maintaining of source program on mass storage for modification and recompilation, a means of modifying parameters and program in symbolic machine language form in core, or other alternate proposals. The operator should also have the capability of changing parameters and information displayed on strip chart recorders from the digital computer. (The hybrid programmer must also be able to modify the analog computer which is controlled by the digital computer.)

5.1.2 Scientific Digital Computation

The system must support general purpose scientific computation. The standard language utilized will be Fortran IV. The system must allow programs that can effectively utilize 48K of core storage.

5.1.3 Integrated Software

Due to the variety of uses of the hybrid facility, a variety of programming tools are required. The effectiveness of these tools is in the large part dependent on their ability to be integrated at the object level to form common programming systems. A great deal of emphasis will be placed on this ability to utilize all programming languages furnished in single programming systems.

5.2 Operational Philosophy

This section of the proposal will be used by the vendor to express his total programming system concept for a hybrid facility. Several topics are discussed to give an indication of the types of concepts that should be considered. The vendor should present his system concepts, where he stands in providing these capabilities, and what kind of a commitment has been made by the vendor in the hybrid and simulation software field. The vendor

may also wish to indicate his willingness to update both software and hardware when major breakthroughs in the state of the art occur.

5.2.1 Basic Operating System

The basic system must be able to handle any type jobs indicated in the operating requirements section. However, in this mode of operation, the configuration of the digital and analog computers will be determined by the operator and equipment will be assigned as required to process the different type jobs. In this mode of operation, the allocation of memory between the digital computers will be made by the operator and the appropriate monitor systems will be loaded into the digital computer. In a large single hybrid problem, each digital computer will operate under its own programming system with only the minimum capability of core overlap required for data transfer. When operating as a digital computer, for normal scientific processing, the system will have the capability of operating as two digital computers or operating as a large digital computer using a single processor. The system must be able to process with a single processor programs which require 48K of core.

5.2.2 Time Sharing Software

Because of the very nature of hybrid computation, it well lends itself to a time-shared software system. Most programs operating in a hybrid system with analog computers are only operating a few hours a day, however, the programs must appear to be functioning continuously at the request of the analog computer operator. However, between runs the analog computer operator will be making modifications to his program and parameters. During this time, the digital computer should be assigned background digital programming tasks. To do this effectively, a time sharing program system is desirable. To effectively do time sharing, computer hardware is required with built-in storage protection to insure the integrity of the system. In a design system such as a hybrid computational laboratory, much time is spent in program debugging. Due to the problems in hybrid programming debugging and in the schedules required in digital programming debugging, on-line debugging is required. The only effective way to allow for on-line programming

debugging features without incurring excessive costs, is by an effective time sharing system. The programmer doing the on-line debugging will share the digital computer much as an analog programmer will share the digital computer in a hybrid program. When the digital programmer wishes to have parameters displayed or a breakpoint placed in his program, the operating system must be able to temporarily place his program on a mass storage and continue operating on background jobs. Certain requirements are placed on the programming system in a hybrid programming mode that aren't apparent in most time shared systems. Most time sharing systems are built around the philosophy that as much processing must take place in the digital computer as possible, and the only goal is efficient use of the digital computer. However, in the hybrid processing mode, the digital computer must process analog interrupts in a high priority status to insure that the digital computation is completed within the real time requirements of the system. This problem of computation in real time increases the sophistication of the required time sharing system. The main goal of the time sharing system in the hybrid programming facility will be to effectively utilize the digital computers when the analog computers are placed in a hold status or when on-line programming debugging is delayed waiting for a programming decision. Some digital processing may also take place on a low priority basis during hybrid runs if core space is available.

5.2.3 Maintenance in a Time Sharing Mode

Due to the largeness of the hybrid system, effective maintenance tools must be available for trouble shooting and standard maintenance of the hybrid facility in a modular fashion. This capability is a requirement as far as the interface equipment and the analog computers are concerned. The capability is a highly desirable feature in the digital area. The maintenance routines written for the interface and analog computers should be written as time shared routines under the standard operating system. This will allow standard calibrations and trouble shooting of analog computers to take place fully utilizing the digital computer without

interferring with the operation of the rest of the system. The vendor will include a table which indicates the effect of the loss of each piece of equipment on the total system.

5.3 Software Packages

The software packages outlined in the following sub-paragraphs will be commented upon by the vendor. The vendor will indicate whether he will furnish the software packages or whether he takes exception to each package. Information on the organization of each program and how it fits into the vendor's software system will be presented.

5.3.1 Executive

The vendor will describe his Executive system and indicate its capabilities as an effective job processing tool.

5.3.1.1 Job Processing

The vendor will comment on the control information required to submit a job under his Executive system.

5.3.1.2 Input-Output Organization

A complete description of the input-output organization and the algorithms used in assigning equipment will be presented.

5.3.1.3 Priority Interrupt Handling

The vendor will indicate what facility is in the Executive for handling priority interrupts.

5.3.1.4 Time Shared Processing

The proposal will contain a description of the capability of his Executive as a time sharing monitor. He will discuss program priority assignment, priority interrupt processing, and use of time sharing hardware.

5.3.1.5 Program Debugging Aids

The vendor will completely discuss the program debugging aids furnished as standard debugging tools in digital scientific computation.

5.3.2 Hybrid Executive

The Hybrid Executive and its relationship to the digital executive shall be described.

5.3.3 Hybrid Debugging

A sophisticated hybrid debugging system will be developed for the

hybrid laboratory. The vendor should indicate his capability in providing this system. For example, the hybrid programmer, through the use of a CRT charactron tube or typewriter could be able to communicate to the debugged system to indicate the instructions from which he wishes response. The program undergoing checkout could be maintained on the mass memory at the source level. The operator could have the capability of scanning this program and having desired sections of the program displayed on the CRT tube.

Modifications to this program will be able to be made and the operator will be able to determine if this is a temporary modification for test, or a permanent modification to the source program. At the request of the operator, the system will recompile the operating program and load the function, reset the analog computer and be prepared to start. Simple modifications such as parameter changes, will be made also from the console. A complete tabulation of all parameter changes will be made and recorded and a summary for each run listed at the request of the operator. The operator will have the option of making temporary parameter changes or having these changes included at the source level. The operator also may wish to run digital checks on his simulation. To do this, he will have the option of maintaining on the mass memory, a source level digital simulation of the analog program of which he is running. The hybrid programmer may run check solutions to determine proper scaling and check for proper setup of his analog computers.

5.3.4 Request Package

The request package will give the console programmer the ability to make adjustments to his program from the on-line typewriter or the program checkout console. This package will include normal computational routines such as sine, cosine, sq. root, etc. and the ability to generate and effect simple arithmetic calculations. The request package will also allow the setting of analog pots and the readout of analog computer parameters.

5.3.5 Fortran IV

Fortran IV will be the standard language for pure digital simulations in the hybrid simulation facility. Standard ASA Fortran IV is a requirement. Fortran IV compatible with IBM 7094 Fortran IV

is a desirable feature. The vendor will indicate in his proposal any language incompatibilities outside of normal control cards between his Fortran IV compiler and IBM 7094 Fortran IV compiler.

5.3.6 Assembler

The vendor will provide the specifications for his standard machine language assembler. He will indicate all macro-generating capabilities or other features of his assembler. A description of the cards generated as output of the assembler program for the loader will also be provided. If the standard assembler program generates card formats which are different from other compilers in the system a description of these differences will be made.

5.3.7 Real Time Fortran

Fortran will also be used for simulation problems. This Fortran may be a simplified version of Fortran IV or may include all the capabilities of Fortran IV. The real time Fortran will have the capability of multi-level operation, where different Fortran subroutines are being executed on a priority basis. The vendor will indicate his approach to the problems of recurrsive subroutines and will give a complete description of how this problem is handled by the compiler. He will also indicate what additions to the language have been made for the special functions found in the analog computer, such as data conversion, pot set, and patchboard readout. He will also indicate how the Fortran operates with standard peripheral units without interferring with the requirements of real time computation.

5.3.8 Simulation Languages

The vendor will indicate the availability of simulation languages. These simulation languages will be evaluated according to the following categories:

1. Adaptability to hybrid computation
2. Ease of use by persons normally accustomed to block organization type programs
3. The ability to integrate simulation compiled routines into routines compiled on other compilers and assemblers such as Fortran
4. The flexibility in using the system as a pure digital simulation tool

5. The effectiveness of the hands on capability in operation familiar in hybrid and analog computation.

5.3.9 Analog Program Check

The analog check program allows the analog or hybrid programmer to check his patched wiring and as a component check of the hybrid computer. The vendor should describe the input of his program check routine, whether the check routine can provide a static or a dynamic check, the compatibility between the language of describing the analog check and the language required by his simulation language.

5.3.10 Computer Diagnostic

The computer and all its peripheral equipment will be delivered with an effective diagnostic system. If a time shared system is proposed, the vendor should discuss the effectiveness of his diagnostic system operating in a time shared mode.

5.3.11 Interface Diagnostic

The vendor should give a complete description of the interface diagnostic. This should include dynamic checks of ADL and DAL lines, in close up tests, the proper functioning of control and status lines, the proper functioning of free interrupt lines.

5.3.12 Analog Computer Diagnostic

The vendor will discuss the programming required to effectively maintain the analog computers.

5.3.13 Installation and Checkout

Programs will be required for installation and checkout of the interface and the analog computers.

5.3.14 Acceptance Tests

The vendor will discuss the software required for acceptance tests of the digital computer, interface equipment, and the analog computers.

5.3.15 Disc Oriented Software

The vendor will completely describe his capability of providing disc oriented software. This will include a description of the Executive's disc organization, and the way in which the Executive assigns and maintains information on the disc. The vendor will

indicate how effectively he uses the random access capability of the disc in loading programs. The vendor will also indicate how standard scratch tape type of operations are handled utilizing a disc. The vendor should completely discuss any software capability which is mag-tape oriented that will not operate on the disc system.

6.0 Exhibits:

The vendor will furnish the following exhibits to provide the information needed for evaluating machine speed, accuracy, and Fortran language compatibility.

6.1 Fortran Compilations:

Instructions

1. Compile each program (See Appendix) without modification except for changes in control cards. Furnish listings and diagnostics of each program.
2. Modify each program if required to enable programs to be compiled without errors. Include listings and machine language assembly for each program. Document carefully any changes in source program.
3. Programs which are marked for compilation and execution will be run and the output included.

6.2 Library Routines:

The vendor will provide the following information in a table for standard library routines. If both high accuracy for scientific computations and high speed routines for hybrid computations are available, information should be included for both.

Information

1. No. core locations
2. Accuracy
3. Executive time

Library Routines

1. SIN
2. COS
3. SQRT
4. ARC SIN
5. ARC COS
6. ARC TAN

7.0 Card Keypunch

The vendor will include two IBM 026 card keypunchs.

8.0 Bidders Instructions

8.1 Costs and Technical Response

The Bidder will make a response to all sections of the RFP including all options and exceptions. Careful consideration should be made to insure that this includes all equipment except those spelled out in installation requirements.

8.2 The Bidder will include prices for all procurement options including:

- SELL
- LEASE
- RENT
- Maintenance Contract
- Spare Parts Contract

8.3 The Bidder will submit the names and titles of personnel who will be associated with the contract if he is selected, and the percentage of their time available in the following areas:

1. Sales
2. Maintenance
3. Applications
4. Programming

APPENDIX

1. Compile the two following subprograms and furnish information necessary for evaluating execution time. These programs are non-executable.

COMPILE ONLY

```
      SUBROUTINE RUNKUT (XI,XDI,DEL)
      REAL MU
      DIMENSION XI(3),XDI(3),X(4,3),XD(4,3),XDD(4,3)
      MU=62746.8
      DT = DEL
   12 DO 14 J=1,3
      X(1,J)=XI(J)
   14 XD(1,J)=XDI(J)
   18 DELTAT = DT/2.0
      DO 40 I=1,3
      R=SQRT(X(I,1)*X(I,1)+X(I,2)*X(I,2)+X(I,3)*X(I,3))
      DO 20 J=1,3
      XDD(I,J) = -(MU*X(I,J))/R**3
      XD(I+1,J) = XD(1,J)+XDD(I,J)*DELTAT
   20 X(I+1,J) = X(1,J)+XD(I,J)*DELTAT
      IF (I-2) 40,30,40
   30 DELTAT = DT
   40 CONTINUE
      R=SQRT(X(4,1)*X(4,1)+X(4,2)*X(4,2)+X(4,3)*X(4,3))
      DO 50 J= 1,3
      XDD(4,J) = -MU*X(4,J)/R**3
      X(1,J) =X(1,J)+(DT/6.0)*(XD(1,J)+2.0*XD(2,J)+2.0*XD(3,J)+XD(4,J))
   50 XD(1,J) = XD(1,J)+(DT/6.0)*(XDD(1,J)+2.0*XDD(2,J)+2.0*XDD(3,J)
     *+XDD(4,J))
      X(1,1)=X(1,1)+DX
      X(1,2)=X(1,2)+DY
      X(1,3)=X(1,3)+DZ
      XD(1,1)=XD(1,1)+DXD
      XD(1,2)=XD(1,2)+DYD
      XD(1,3)=XD(1,3)+DZD
      DX=DY=DZ=DXD=DYD=DZD=0.
      RETURN
      END
```

FORTRAN

```
      SUBROUTINE CONFIG
         DIMENSION K(20),TV(20),W(20),XCG(20),DW(20),YCG(20)
         DIMENSION ZCG(20),RRX(20),RXCG(20),RRY(20),RYCG(20),RRZ(20)
         DIMENSION RZCG(20),RRXX(20),RRYY(20),RRZZ(20)
         DIMENSION RIXX0(20),RIYY0(20),RIZZ0(20)
     1,  RIXY0(20),RIXZ0(20),RIYZ0(20)
      Q=0.
      DO 1 N=1,NN
    1 Q=Q+K(N)*TV(N)
      WD=Q/ISP
      TBO=WP/WD
      F=(T-TO)/TBO
      DW=0.
      DO 2 N=1,NBD
    2 DW=DW+W(N)
      WB=WO-WP*F-DW
      XCGR=0.
      JIM=NB-NBD
      DO 3 N=1,JIM
    3 XCGR=XCGR+XCG(N)*DW(N)
      XCGB=(XCGO*WO-XCGP*WP-XCGR)/WB
      YCGR=0.
      JIM=NB-NBD
      DO 4 N=1,JIM
    4 YCGR=YCGR+YCG(N)*DW(N)
      YCGB=(YCGO*WO-YCGP*WP-YCGR)/WB
      ZCGR=0.
      JIM=NB-NBD
      DO 5 N=1,JIM
    5 ZCGR=ZCGR+ZCG(N)*DW(N)
      ZCGB=(ZCGO*WO-ZCGP-ZCGR)/WB
      ENTRY UPCON
      XRCG=0
      JIM=NBD+1
      DO 6 N=JIM,NB
    6 XRCG=XRCG+XCG(N)*DW(N)
      YRCG=0.
      JIM=NBD+1
      DO 7 N=JIM,NB
    7 YRCG=YRCG+YCG(N)*DW(N)
      ZRCH=0.
      JIM=NBD+1
      DO 8 N=JIM,NB
    8 ZRCG=ZRCH+ZCG(N)*DW(N)
      XCG=(XCGB*WB+XCGP*WP*(1.-F)+XRCH)/W
      XCG=(YCGB*WB+YCGP*WP*(1.-F)+YRCG)/W
      ZCG=(ZCGB*WB+ZCGP*WP*(1.-F)+ZRCG)/W
      W=WB+WP*(1.-F)+RW
      RW=0.
      JIM=NBD+1
      DO 9 N=JIM,NB
    9 RW=RW+DW(N)
      RPX=XCGP-XCG
      RPY=YCGP-YCG
      RPZ=ZCGP-ZCG
      RPX2=RPX*RPX


      RPY2=RPY*RPY
      RPZ2=RPZ*RPZ
```

```
      RPXX=RPY2+RPZ2
      RPYY=RPX2+RPZ2
      RPZZ=RPX2+RPY2
      RCGX=XCG-XCG0
      RCGY=YCG-YCG0
      RCGZ=ZCG-ZCG0
      RX2=RCGX*RCGX
      RY2=RCGY*RCGY
      RZ2=RCGZ*RCGZ
      RCGXX=RY2+RZ2
      RCGYY=RX2+RZ2
      RCGZZ=RX2+RY2
      DO 10 N=1,NR
      RRX(N)=RXCG(N)-XCG
      RRY(N)=RYCG(N)-YCG
      RRZ(N)=RZCG(N)-ZCG
      RX2=RRX(N)*RRX(N)
      RY2=RRY(N)*RRY(N)
      RZ2=RRZ(N)*RRZ(N)
      RRXX(N)=RY2+RZ2
      RRYY(N)=RX2+RZ2
10    RRZZ(N)=RX2+RY2
      RIXX=RIYY=RIZZ=RIXY=RIXZ=RIYZ=0.
      DO 11 N=1,NBD
      RIXX=RIXX+DW(N)*RRXX(N)*G+RIXX0(N)
      RIYY=RIYY+DW(N)*RRYY(N)*G+RIYY0(N)
      RIZZ=RIZZ+DW(N)*RRZZ(N)*G+RIZZ0(N)
      RIXZ=RIXZ+DW(N)*RRX(N)*RRZ(N)*G+RIXZ0(N)
11    RIYZ=RIYZ+DW(N)*RRY(N)*RRZ(N)*G+RIYZ0(N)
      TU1=TU
      TU=T
      DT=TU-TU1
      DIXX=(IXX-IXX1)/DT
      DIYY=(IYY-IYY1)/DT
      DIZZ=(IZZ-IZZ1)/DT
      DIXY=(XIXY-XIXY1)/DT
      DIXZ=(XIXZ-XIXZ1)/DT
      DIYZ=(XIYZ-XIYZ1)/DT
      D=XIXX*XIYY*XIZZ+2.*XIXY*XIXZ*XIYZ-XIXX*XIYZ*XIYZ-XIYY*XIXZ*XIXZ-X
     1IZZ*XIXY*XIXY
      XIXX=(XIYY*XIZZ-XIYZ*XIYZ)/D
      XIYY=(XIXX*XIZZ-XIXZ*XIXZ)/D
      XIZZ=(XIZZ*XIYY-XIXY*XIXY)/D
      XIXY=(XIXZ*XIYZ-XIXY*XIZZ)/D
      XIXZ=(XIXY*XIYZ-XIYY*XIXZ)/D
      XJYZ=(XIXY*XIXZ-XIXX*XIYZ)/D
      XIXX1=XIXX
      XIYY1=XIYY
      XIZZ1=XIZZ
      XIYY1=XIXY
      XIXZ1=XIXZ
      XIYZ1=XIYZ
      XIXX=XIXX0-RPXX*WP*F*G-RIXX+W*G*RCGXX
      XIYY=XIYY0-RPYY*WP*F*G-RIYY+W*G*RCGYY
      XIZZ=XIZZ0-RPZZ*WP*F*G-RIZZ+W*G*RCGZZ
      XIXY=XIXY0-RPX*RPY*WP*F*G-RIXY+W*G*RCGX*RCGY
      XIXZ=XIXZ0-RPX*RPZ*WP*F*G-RIXZ+W*G*RCGX*RCGZ
      XIYZ=XIYZ0-RPY*RPZ*WP*F*G-RIYZ+W*G*RCGY*RCGZ
      RETURN
      END
```

2. The following program is set up to run on the UNIVAC 1108 computer. Two calls are made to timing routines. Compile and execute these programs.

```
* LID              B101011504  5533  BMH200            JACOBSON 5533  15331967
* MSG JACOBSON D/55-33 B/153 REMOTE
NT FOR MAINP
      DRIVER TO CHECK OUT PCIRCL.
    1 READ (5,100)SIGX,SIGY,AMX,AMY,RHOXY,BIGR,ESTD
  100 FORMAT(6E12.8/E12.8)
      WRITE(6,200) SIGX,SIGY,AMX,AMY,RHOXY,BIGR,ESTD
  200 FORMAT( 33H INPUT DATA FOR PCIRCL CHECKOUT      /7E18.8 //)
      CALL ELT1
      CALL PCIRCL(SIGX,SIGY,AMX,AMY,RHOXY,BIGR,PBIGR,EPBIGR,ESTD)
       DIMENSION X(2)
      CALL ELT2(X)
      WRITE (6,400) X
  400 FORMAT(17H  ELAPSED TIME =       A6,A2)
      WRITE (6,300) PBIGR, EPBIGR, ESTD
  300 FORMAT(20H  OUTPUT.  PBIGR =    E18.8, 9H EPBIGR=    E18.8,
     1   12H FOR ESTD =   E18.8)
      GO TO 1
      END
```

```
*IT FOR PCIRCL,PCIRCL                                                    PCIR000
      SUBROUTINE PCIRCL(SIGX,SIGY,AMX,AMY,RHOXY,BIGR,PBIGR,EPBIGR,ESTD) PCIR001
      INTEGRATES BIVARIATE DISTRIBUTION OVER A CIRCLE OF RADIUS BIGR     PCIR002
C     CENTERED AT X=0.,Y=0.                                              PCIR003
C     SIGX= STD. DEVIATION IN X,  AMX = MEAN IN X                        PCIR004
C     SIGY= STD. DEVIATION IN Y,  AMY = MEAN IN Y                        PCIR005
C     RHOXY = CORRELATION COEFFICIENT BETWEEN X AND Y.                   PCIR006
C     PBIGR = PROBABILITY OF BEING INSIDE CIRCLE (OUTPUT)                PCIR007
C     EPBIGR = CONVERGENCE ERROR IN PBIGR AT LAST INTEGRATION (OUTPUT)   PCIR008
C     (ABS(EPBIGR) SHOULD BE LESS THAN ESTD)                             PCIR007
C     ESTD = CONVERGENCE ERROR STD. (IF ESTD INPUT = 0.,-,OR MORE THAN   PCIR009
C      1.E-2,STHEN SETS=ESTD = 1.E-5                                     PCIR010
C                                                                        PCIR011
      COMMON /CKALL/C1,C2,C3,C4,C5,C6                                    PCIR012
      COMMON /VARUV/U,USQ,V,VSQ,UV,SIGU,SIGV                             PCIR013
      RHOXY2 = RHOXY**2                                                  PCIRC14
      IF ( RHOXY2.LT.(1.0)) GO TO 10                                     PCIRC15
      WRITE (6,100) RHOXY                                                PCIRC16
  10C FORMAT(34H  ERROR EXIT FROM PCIRCL, RHOXY=       E16.8    )       PCIRC17
      CALL EXIT                                                          PCIRC18
C     ROTATE TO PRINCIPAL AXES OF ELLIPSE OF ERROR                       PCIRC19
   10 SIGXSQ = SIGX**2                                                   PCIRC20
      SIGYSQ = SIGY**2                                                   PCIRC21
      SIGXY  = SIGX* SIGY                                                PCIRC22
      EXY    = 2.*( RHOXY * SIGXY )                                      PCIRC23
      DXY    = SIGXSQ - SIGYSQ                                           PCIRC24
      IF (DXY.GT.(0.)) GO TO 1                                           PCIRC25
      IF (DXY.LT.(0.)) GO TO 1                                           PCIRC26
      PSI=.78539816
      GO TO 2                                                            PCIRC28
    1 TAN2PS = EXY / DXY                                                 PCIRC29
C     PSI = ROTATION ANGLE FROM X,Y   AXES TO  U,V  AXES                 PCIRC30
      PSI = 0.5* ATAN(TAN2PS)                                            PCIRC31
    2 SPSI = SIN(PSI)                                                    PCIRC32
      CPSI = COS(PSI)                                                    PCIRC33
      SPSISQ = SPSI**2                                                   PCIRC34
      CPSISQ = CPSI**2                                                   PCIRC35
      SCPSI  = SPSI*CPSI                                                 PCIRC36
      SIGUSQ = SIGXSQ*CPSISQ + SIGYSQ*SPSISQ + EXY* SCPSI                PCIRC37
      SIGVSQ = SIGXSQ*SPSISQ + SIGYSQ*CPSISQ - EXY* SCPSI                PCIRC38
C     SIGU = STD. DEVIATION IN U                                         PCIRC39
      SIGU = SQRT( SIGUSQ)                                               PCIRC40
C     SIGV = STD. DEVIATION IN V                                         PCIRC41
      SIGV = SQRT( SIGVSQ)                                               PCIRC42
      SIGUV = SIGU*SIGV                                                  PCIRC43
C     AMU = MEAN IN U                                                    PCIRC44
      AMU = AMX* CPSI + AMY*SPSI                                         PCIRC45
C     AMV = MEAN IN V                                                    PCIRC46
      AMV =-AMX* SPSI + AMY*CPSI                                         PCIRC47
      AMUSQ = AMU**2                                                     PCIRC48
      AMVSQ = AMV**2                                                     PCIRC49
      AMUV  = AMU*AMV                                                    PCIRC50
      DATA PI2 /6.28318531/                                              PCIRC51
      CALCULATE CONSTANTS FOR PROBABILITY DENSITY IN U AND V.            PCIRC52
      C1 = 1./ (PI2* SIGUV)                                              PCIRC53
      C2 = -0.5*(AMUSQ/SIGUSQ + AMVSQ /SIGVSQ )                          PCIRC54
      C3 =  AMU / SIGUSQ                                                 PCIRC55
```

```
      C4 = -0.5 / SIGUSQ                                                PCIRC56
      C5 =  AMV / SIGVSQ                                                PCIRC57
      C6 = -0.5 / SIGVSQ                                                PCIRC58
      F(U,V) = C1*EXP(C2 + C3*U + C4*USQ + C5*V + C6*VSQ )              PCIRC59
C             = PROBABILITY DENSITY IN U AND V                          PCIRC60
C     SET UP ESTD                                                       PCIRC61
      IF (ESTD.LT.(0.))GO TO 3                                          PCIRC62
      IF (ESTD.EQ.(0.))GO TO 3                                          PCIRC63
      IF (ESTD.GT.(1.E-2))GO TO 3                                       PCIRC64
      GO TO 4                                                           PCIRC65
    3 ESTD = 1.E-5                                                      PCIRC66
C     INTEGRATE  F(U) FROM  U = -BIGR TO U= +BIGR TO GET PROBABILITY    PCIRC67
    4 CALL SUMU( PBIGR,EPBIGR,ESTD,BIGR)                                PCIRC68
      RETURN                                                            PCIRC69
      END                                                               PCIRC70
```

```
*IT FOR SUMU,SUMU                                                    SUMU000
      SUBROUTINE SUMU(FC,EFC,ESTD,BIGR)                              SUMU001
      SUBROUTINE FOR INTEGRATING PROBABILITY DENSITY FOR U FROM      SUMU002
C     - BIGR TO + BIGR                                               SUMU003
C                                                                    SUMU004
      COMMON /CKALL/C1,C2,C3,C4,C5,C6                                SUMU005
      COMMON /VARUV/ U, USQ, V,VSQ,UV,SIGU,SIGV                      SUMU006
      DIMENSION HC(1025),IFLAG(1025),NC(9)                           SUMU007
      DATA (NC(K),K= 1,9)/4,8,16,32,64,128,256,512,1024/             SUMU008
C     SET UP INTEGRATION INTERVAL AND LIMITS                         SUMU009
      C = BIGR + BIGR                                                SUMU010
      CLL = - BIGR                                                   SUMU011
      CUL = + BIGR                                                   SUMU012
      CON = C1                                                       SUMU013
C     CLEAN UP FOR NEW INTEGRATION                                   SUMU014
      DO 500 J= 1,1025                                               SUMU015
      IFLAG(J) = 0                                                   SUMU016
  500 HC(J) = 0.                                                     SUMU017
C     MAXIMUM STEP SIZE CHECK                                        SUMU018
      DT = C/ 1024.                                                  SUMU019
      PMIN = SIGU                                                    SUMU020
      IF(PMIN.LT.(2.*DT)) GO TO 10                                   SUMU021
      GO TO 20                                                       SUMU022
   10 PMIN = 2.* DT                                                  SUMU023
C     CALCULATE 5-POINT NEWTON-COTES INTEGRATION COEFFICIENTS        SUMU024
   20 CINT1 = (C *14.)/180.                                          SUMU025
      CINT2 =(C *64.)/180.                                           SUMU026
      CINT3 =(C* 24.)/180.                                           SUMU027
      SC= 0.                                                         SUMU028
      ESC= 1.                                                        SUMU029
      FC= 2.                                                         SUMU030
      EFC=3.                                                         SUMU031
      DO 100 K=1,9                                                   SUMU032
      N = NC(K)                                                      SUMU033
      ISTEP = 1024/N                                                 SUMU034
      Y = NC(K)                                                      SUMU035
      PSTEP = C /Y                                                   SUMU036
      IF (PSTEP.GT.PMIN) GO TO 100                                   SUMU037
  600 IF (N.GT.1025) GO TO 300                                       SUMU038
      NS = N+1                                                       SUMU039
      DO 200 J=1,NS                                                  SUMU040
      JSTEP = ISTEP*(J-1)+ 1                                         SUMU041
      I = IFLAG (JSTEP)                                              SUMU042
      IF (I.EQ.1) GO TO 200                                          SUMU043
      Z = J-1                                                        SUMU044
      T = Z* PSTEP + CLL                                             SUMU045
C     COMPUTE FUNCTIONS OF U FOR INTEGRATION                         SUMU046
      U = T                                                          SUMU047
      USQ = U**2                                                     SUMU048
      FEXPU = C3*U + C4* USQ + C2                                    SUMU049
C     INTEGRATE CHORD OF CIRCLE OF RADIUS BIGR FOR GIVEN U  ALONG V  SUMU050
      CALL SUMCHV(GUV,EGUV,FEXPU,ESTD,BIGR)                          SUMU051
      HC(JSTEP) = GUV                                                SUMU052
  200 IFLAG(JSTEP) = 1                                               SUMU053
C     INTEGRATION PORTION USING FIVE-POINT NEWTON-COTES FORMULA      SUMU054
      M = N/4                                                        SUMU055
      MSTEP = 4* ISTEP                                               SUMU056
```

```
      SUM = 0.                                                                  SUMU057
      DO 400 L= 1,M                                                             SUMU058
      LSTEP1 = MSTEP* (L-1) + 1                                                 SUMU059
      LSTEP2 = LSTEP1 + ISTEP                                                   SUMU060
      LSTEP3 = LSTEP2 + ISTEP                                                   SUMU061
      LSTEP4 = LSTEP3 + ISTEP                                                   SUMU062
      LSTEP5 = LSTEP4 + ISTEP                                                   SUMU063
      DSUM= CINT1* (HC(LSTEP1) + HC(LSTEP5))                                    SUMU064
     1 + CINT2*( HC(LSTEP2) + HC(LSTEP4))  +  CINT3* HC(LSTEP3)                 SUMU065
  400 SUM = SUM + DSUM                                                          SUMU066
      A = M                                                                     SUMU067
      FC = SUM* CON/A                                                           SUMU068
      EFC = (FC - SC)/FC                                                        SUMU069
      IF(ABS(EFC).LT.ESTD) GO TO 300                                            SUMU070
      SC = FC                                                                   SUMU071
  100 ESC = EFC                                                                 SUMU072
  300 RETURN                                                                    SUMU073
      END                                                                       SUMU074
```

```
*IT FOR SUMCHV,SUMCHV                                                  SUMCH00
      SUBROUTINE SUMCHV (FC,EFC,FEXPU,ESTD,BIGR)                       SUMCH01
      INTEGRATES OVER CHORD OF CIRCLE FOR GIVEN U ALONG V              SUMCH02
C     FROM -SQRT(BIGR**2  -USQ) TO + SQRT(BIGR**2 - USQ)               SUMCH03
C                                                                      SUMCH04
      COMMON /CKALL/C1,C2,C3,C4,C5,C6                                  SUMCH05
      COMMON /VARUV/U,USQ,V,VSQ,UV,SIGU,SIGV                           SUMCH06
      DIMENSION HC(1025),IFLAG(1025),NC(9)                             SUMCH07
      DATA(NC(K),K= 1,9)/4,8,16,32,64,128,256,512,1024/                SUMCH08
C     SET UP INTEGRATION  INTERVAL AND LIMITS                          SUMCH09
      CULSQ = BIGR**2 - USQ                                            SUMCH10
      IF(CULSQ.LT.(0.0))GO TO 700                                      SUMCH11
      IF(CULSQ.GT.(0.0))GO TO 701                                      SUMCH12
  700 FC = 0.                                                          SUMCH13
      EFC = 0.                                                         SUMCH14
      GO TO 300                                                        SUMCH15
  701 CUL = SQRT(CULSQ)                                                SUMCH16
      CLL = - CUL                                                      SUMCH17
      C   =  CUL - CLL                                                SUMCH18
      CON = 1.                                                         SUMCH19
C     WIPE UP CORE BEFORE INTEGRATION                                  SUMCH20
      DO 500  J = 1,1025                                               SUMCH21
      IFLAG(J)= 0                                                      SUMCH22
  500 HC(J) = 0.                                                       SUMCH23
      DT = C /1024.                                                    SUMCH24
C     MAXIMUM STEP SIZE CHECK.                                         SUMCH25
      PMIN = SIGV                                                      SUMCH26
      IF(PMIN.LT.(2.*DT)) GO TO 10                                     SUMCH27
      GO TO 20                                                         SUMCH28
   10 PMIN = 2.* DT                                                    SUMCH29
C     CALCULATE 5-POINT NEWTON-COTES INTEGRATION COEFFICIENTS          SUMCH30
   20 CINT1 = (C * 14.)/ 180.                                          SUMCH31
      CINT2 = (C * 64.)/ 180.                                          SUMCH32
      CINT3 = (C * 24.)/ 180.                                          SUMCH33
      SC = 0                                                           SUMCH34
      ESC= 1.                                                          SUMCH35
      FC = 2.                                                          SUMCH36
      EFC= 3.                                                          SUMCH37
      DO 100 K= 1,9                                                    SUMCH38
      N = NC(K)                                                        SUMCH39
      ISTEP = 1024/N                                                   SUMCH40
      Y = NC(K)                                                        SUMCH41
      PSTEP = C /Y                                                     SUMCH42
      IF (PSTEP.GT.PMIN) GO TO 100                                     SUMCH43
  600 IF (N. GT.1025) GO TO 300                                        SUMCH44
      NS = N+1                                                         SUMCH45
      DO 200 J= 1,NS                                                   SUMCH46
      JSTEP = ISTEP* (J-1) + 1                                         SUMCH47
      I = IFLAG(JSTEP)                                                 SUMCH48
      IF (I.EQ. 1) GO TO 200                                           SUMCH49
      Z = J-1                                                          SUMCH50
      T = Z* PSTEP + CLL                                               SUMCH51
      COMPUTE FUNCTIONS OF V FOR INTEGRATION                           SUMCH52
      V = T                                                            SUMCH53
      VSQ = V**2                                                       SUMCH54
      FEXPUV = FEXPU + C5*V + C6*VSQ                                   SUMCH55
C     HC = F(U,V) /C1                                                  SUMCH56
```

```
      HC(JSTEP)=      EXP(FEXPUV)                                              SUMCH57
  20C IFLAG(JSTEP) = 1                                                         SUMCH58
      INTEGRATION PORTION USING FIVE-POINT NEWTON-COTES FORMULA                SUMCH59
      M= N/4                                                                   SUMCH60
      MSTEP = 4* ISTEP                                                         SUMCH61
      SUM = 0.                                                                 SUMCH62
      DO 400  L =1,M                                                           SUMCH63
      LSTEP1  = MSTEP*(L-1) + 1                                                SUMCH64
      LSTEP2  = LSTEP1 + ISTEP                                                 SUMCH65
      LSTEP3  = LSTEP2 + ISTEP                                                 SUMCH66
      LSTEP4  = LSTEP3 + ISTEP                                                 SUMCH67
      LSTEP5  = LSTEP4 + ISTEP                                                 SUMCH68
      DSUM = CINT1*(HC(LSTEP1) + HC(LSTEP5))                                   SUMCH69
     1 + CINT2*( HC(LSTEP2) + HC(LSTEP4))  + CINT3 * HC(LSTEP3)                SUMCH70
  400 SUM = SUM + DSUM                                                         SUMCH71
      A = M                                                                    SUMCH72
      FC = SUM* CON /A                                                         SUMCH73
      EFC = (FC - SC) /FC                                                      SUMCH74
      IF(ABS(EFC).LT.ESTD) GO TO 300                                           SUMCH75
      SC = FC                                                                  SUMCH76
  100 ESC= EFC                                                                 SUMCH77
  300 RETURN                                                                   SUMCH78
      END                                                                      SUMCH79
```

```
'L XQT MAINP
  4.+          3.+          2.+          1.+          +0.5+        2.+
  1.      -07
   1.+          1.+          0.+          0.+          0.+          1.+
  1.      -06
   1.+          1.+          2.+          0.+          0.+          3.+
  1.      -04
   1.+          0.4+         2.+          3.+          0.+          5.+
   2.+
    1.+          1.+                                                .5+
  1.      -06
' FIN
```

INPUT DATA						OUTPUT DATA			
σ_X Std. Dev. in X	σ_Y Std. Dev. in Y	α_X Mean in X	α_Y Mean in Y	ρ_{XY} Corrlation Betw. X & Y	R Target Circle Radius	ESTD Convergence Error Std.	P ($0<r<R$) Circular Hit Probability	ϵ_P Last Convergence Error	Univac 1107 Run Time (Sec)
1	1	0	0	0	0.5	$1.X10^{-5}$	0.11750	$0.19x10^{-4}$	19
						$1X10^{-6}$	0.117502	$0.19X10^{-4}$	24
					1.	$1.X10^{-5}$	0.39347	$0.15X10^{-4}$	27
						$1\ X10^{-6}$	0.39347	$0.15X10^{-4}$	32
1	1	+2	0	0	3	$1X10^{-4}$	0.78562	$0.48X10^{-4}$	8
						$1X10^{-5}$	0.78563	$0.58X10^{-5}$	43
4	3	+2	+1	0.5	2	$1.X10^{-5}$	0.15214	$0.20X10^{-4}$	28
						$1X10^{-6}$	0.15214	$0.20X10^{-4}$	36
1	0.4	+2	+3	0	5	$1X10^{-5}$	0.9693	$-0.28X10^{-5}$	12

TABLE I - NUMERICAL RESULTS OF CIRCULAR PROBABILITY PROGRAM

DEFINITION OF TERMS USED TO SPECIFY GENERAL-PURPOSE ANALOG COMPUTERS

and

METHODS OF MEASUREMENT

This document is being published by SCi as a step toward the development of an American and, hopefully, an International standard covering general-purpose analog computers. Participation of all interested organizations and companies will be sought through the machinery of the American Standards Association. Meanwhile, comments and suggestions will be welcomed by committee chairman J. E. Sherman, D59-15, B 102, P. O. Box 504, Sunnyvale, California.

Left to right: R. D. Blosser, W. N. McLean, J. E. Sherman, W. Comley, J. E. Reich

INTRODUCTION

In recent years it has become increasingly obvious that there are ambiguities in some of the terms which are commonly used to specify components and performance criteria of analog computers. In an effort to bring some uniformity to this area, Dr. Hans F. Meissinger, Chairman of the Western Simulation Council, appointed a committee to decide upon a set of standard definitions of terms used in specifying analog computers. This committee was appointed at a meeting of the Steering Committee of the Western Simulation Council at Norair, Division of Northrop Aircraft, on November 10, 1960. The committee comprises the following people:

J. E. Sherman, *Chairman*
Lockheed Missiles & Space Company

W. N. McLean
North American Aviation

J. E. Reich
Space Technology Laboratories, Inc.

W. Comley
Douglas Aircraft Company

R. D. Blosser
Autonetics

The primary goal of the committee is to define certain terms commonly used in specifying analog computers. To define some of these terms, it is necessary to describe the methods by which certain measurements should be made. Therefore, the definitions are divided into two parts: (1) Definitions of Terms Used to Specify Analog Computers, and (2) Measurement Procedures.

Examples of the ambiguities which led to the establishment of the committee are the term *accuracy* as applied to analog computers, the definition of an electronic multiplier, etc.

One often hears of an analog computer's having an "accuracy of .01%." This is obviously an erroneous statement. In truth, the statement should read that the computer has "an error of less than .01%," or the computer has "an accuracy of 99.99%." Ignoring semantics for a moment, it has long been the practice of the industry to claim "an accuracy of .02%" for electronic multipliers. When it comes time to measure the performance of the component in question, it develops that the interpretation put upon this figure by the manufacturers is .02% of full scale ($\pm$100 volts) and is then interpreted by them as being $\pm$40 millivolts. The reasoning they use in arriving at this conclusion is that it is possible for the peak-to-peak value of the signal to be 200 volts, and they then say that .02% of 200 volts is 40 millivolts.

Table of Contents

However, the point that they choose to suppress is that the term ±40 millivolts is really 80 millivolts peak-to-peak, which is .04% of the peak-to-peak signal value. Further, these specifications apply to the multiplier only when the inputs are essentially stationary. There is no convenient or commonly accepted method of specifying the dynamic performance of the multiplier.

When the term *electronic multiplier* is used, it is sometimes not clear exactly what is meant. Does the device merely require inputs of *X* and *Y* from sources of any impedance? Or does it require inputs of both plus and minus *X* and plus and minus *Y*, all from low-impedance sources? Can the output be fed directly to a low-impedance termination, or must it be terminated in a high impedance? It is clear there may be a difference of five amplifiers between the two cases.

It is in an effort to clarify these and like situations that the Western Simulation Council Committee on Uniform Specifications for Analog Computer Performance was formed. The definitions proposed by the Committee have been discussed with technical representatives from several of the leading manufacturers of analog computing equipment.*

The following definitions describe not only terms used in identifying analog computing components, but also terms used in identifying analog computer performance. All measurements which are made to determine analog computer performance should be made under the manufacturer's specified ambient conditions and environment. Further, the performance of the analog computer should remain within the specifications throughout a nine-hour period following setup according to the manufacturer's suggested normal procedures. This means, for example, that a time division electronic multiplier which is balanced and nulled at 8:00 a.m. should meet its specified performance criteria anytime during the following nine hours (until 5:00 p.m.) without additional balancing or adjustment procedures.

All analog computer performance measurements are to be made with the unit under test in a computer cabinet and at the normal input and output terminals of the unit. In the case of a computer using a removable patchboard, this means that all measurements should be made at the patchboard.

All performance data which are presented in graphical form as a function of frequency should be presented on 8½" x 11" three-cycle semilog paper. If the frequency domain of interest is greater than three decades, additional sheets of paper showing three decades each should be used.

*Applied Dynamics, Inc., Beckman/Berkeley Division, Computer Systems, Inc., Electronic Associates, Inc., Reeves Instrument Co.

This set of definitions is not complete. There are a number of terms which have not yet been defined. The terms which have been defined are those generally associated with the description and performance of the following analog computing components:

Arbitrary Electronic Function Generators
Electronic Multipliers
Electronic Resolvers
Electronic Sinusoid Generators
Servo Multipliers
Summing Amplifiers

Yet to be covered by a similar set of terms are the following components:

Computing Consoles
Digital Voltmeters
Monitoring Devices
Potentiometers
Power Supplies
Random-Noise Generators
Relays
Time-History Recorders
X-Y Plotting Boards

Also to be defined are terms concerned with the following types of computation:

Iterative Computation
Repetitive-Operation Computation

and such specialized terms as:

Algebraic Loop Gain
Stability Margin

The complete list of terms defined in this section of the definitions is as follows:

Component, Computer
Current, Maximum Input
Current, Maximum Output
Curve, Standard Straight-Line
Drift
Element, Circuit
Element, Computing
Element, Shared-Circuit
Error, Setup
Error, Static
Error, Total
Frequency Response, Amplitude
Frequency Response, Phase
Function Generator, Arbitrary Electronic
Ideal
Impedance, Input
Impedance, Output (Source)
Load, Standard Input
Load, Standard Output
Multiplier, Electronic
Multiplier, Servo
Noise
R
Recovery Time, Overload
Resolver, Electronic (Forward-Inverse)
Response, Transient
Scale Factor, Output
Sinusoid Generator, Electronic
Voltage, Maximum Output

ELEMENT, CIRCUIT

Any piece of electronic hardware which is used to make up a computer component or computing element. Some examples of circuit elements are vacuum tubes, resistors, capacitors, transistors, relays, etc.

ELEMENT, COMPUTING

The term *computing element* refers specifically to those components which perform the mathematical operations required for problem solution and as such are shown explicitly in computer diagrams, e.g., summing amplifiers, integrating amplifier, multipliers, etc.

ELEMENT, SHARED-CIRCUIT

A shared-circuit element is a single element which has dual properties, and these properties are used, either simultaneously or on a time-shared basis, in two or more computer components or computing elements (e.g., a chopper in a quad amplifier which modulates the D-C offset for two or more of the amplifiers in the quad chassis; a dual triode, one half of which is used in each of two computer components; a multipole relay which is used in the Hold-Operate circuits of two or more integrating amplifiers; a multipole relay which is used to switch the reference voltage to two or more potentiometers in a servo-set potentiometer system). Specifically *not* included are such computer components as power supplies which supply more than one amplifier, a rack which contains a number of computer components, etc.

ERROR, SETUP

Arbitrary Electronic Function Generator: Maximum departure from the ideal output signal under conditions of a stationary input signal. (See Methods of Measurement.)

ERROR, STATIC

Electronic Sinusoid Generator: The difference between the actual output of the electronic sinusoid generator and its ideal output (as obtained from a trigonometric table) for a stationary input θ. The difference shall be plotted as a function of θ and expressed in millivolts and as a percentage of R.

Electronic Multiplier, Servo Multiplier, Summing Amplifier: That value which the total error approaches asymptotically as the frequency approaches zero.

ERROR, TOTAL

The maximum instantaneous departure from the ideal output. (See Methods of Measurement.)

FREQUENCY RESPONSE, AMPLITUDE

The output-input ratio $\frac{\text{modulus } e_o}{\text{modulus } e_i}$ plotted as a function of frequency. (See Methods of Measurement.)

FREQUENCY RESPONSE, PHASE

The phase angle α plotted as a function of frequency. The angle α defined by the equation

$$\alpha^\circ = 360\ t/T$$

where t and T have the meanings illustrated below.

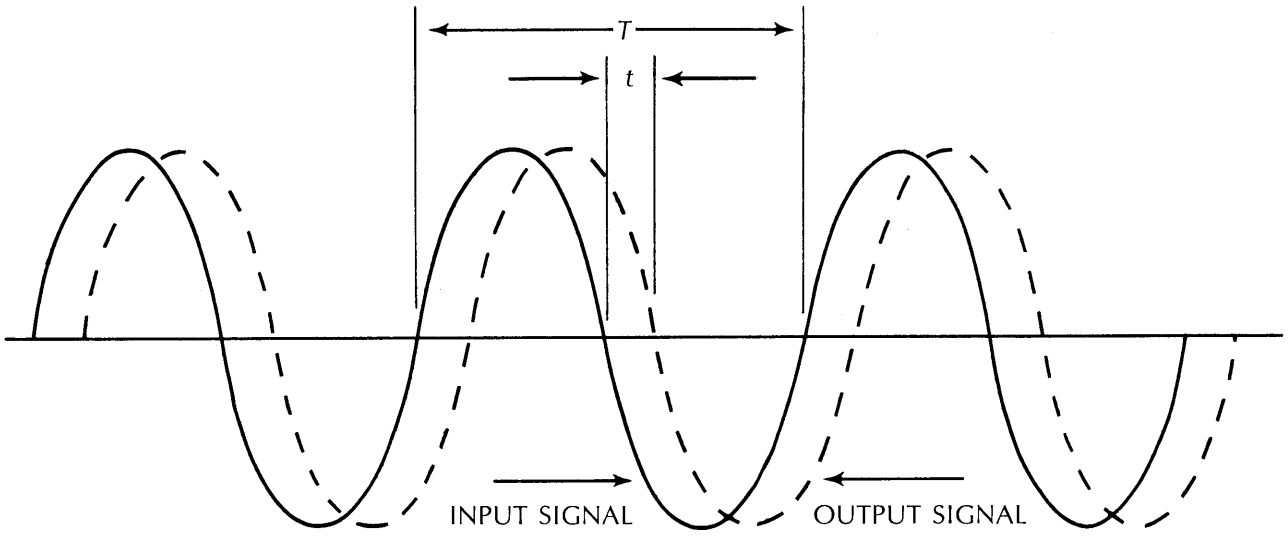


Figure D-2

(See Methods of Measurement.)

Class III: A computing element which requires the addition of three computing amplifiers to meet the requirements for a Class 0 electronic multiplier.

Class IV: A computing element which requires the addition of four computing amplifiers to meet the requirements for a Class 0 electronic multiplier.

Class V: A computing element which requires the addition of five computing amplifiers to meet the requirements for a Class 0 electronic multiplier.

MULTIPLIER, SERVO

An electro-mechanical computing element (consisting of a servo-motor, servo amplifier, and two or more potentiometers mechanically connected to the motor shaft) which accepts two or more signals (either stationary or non-stationary) from a low impedance source and furnishes a high impedance output (e.g., a potentiometer) which is related to the input signals according to the mathematical laws of multiplication.

NOISE

The fluctuating voltage above 0.1 cps superimposed on the ideal output. (See Methods of Measurement.)

R

R is the value of the reference voltage in the computing system. When a computing system has a reference voltage of R, it implies that all elements in the computing system have an operating range of at least $-R$ to $+R$.

RECOVERY TIME, OVERLOAD

The time required for the output of a computer element to return to and remain within $\pm 0.0001R$ (or twice its static error, whichever is greater) of its ideal output after being subjected to an overload. (See Methods of Measurement.)

RESOLVER, ELECTRONIC (FORWARD — INVERSE)

An electronic computing element which accepts two signals (either stationary or nonstationary) from a high-impedance source (e.g., a computing potentiometer) and furnishes two low-impedance output signals which are related to the input signals in such a way as to form a coordinate transformation from either polar coordinates to rectangular coordinates or from rectangular coordinates to polar coordinates. A resolver performs both transformations. In a forward resolution (*i.e.*, from polar to rectangular coordinates), the input signals are r and θ and the output signals are $x = r \cos \theta$ and $y = r \sin \theta$.

In inverse resolution, the input signals are x and y and the output signals are

$$r \left(= \sqrt{x^2 + y^2}\right) \text{ and } \theta \left(= \tan^{-1} \frac{y}{x}\right)$$

RESPONSE, TRANSIENT

The output signal of a computing element when a square-wave input signal of peak amplitude 0 to $+KR$ and 0 to $-KR$ is applied to the input of the computing element. (See Methods of Measurement.)

SCALE FACTOR, OUTPUT

Electronic Multiplier in multiply mode: The numerical value of K in the expression

$$e_o = K e_1 e_2$$

where e_o is the output signal and e_1 and e_2 are the input signals. K has units of *volts*$^{-1}$.

Electronic Multiplier in divide mode: The numerical value of K in the expression

$$e_o = K \frac{e_1}{e_2}$$

K has units of *volts*.

Electronic Resolver — forward resolution (polar to rectangular): The value of K in the expression

$$e_o = e_1 \sin K e_2$$

K has units of *degrees per volt*.

Electronic Resolvers—inverse resolution (rectangular to polar): The value of K in the following expressions

$$e_o = \sqrt{e_1^2 + e_2^2}$$

$$e_o = K \tan^{-1} \frac{e_1}{e_2}$$

K has units of *volts per degree*.

SINUSOID GENERATOR, ELECTRONIC

Class 0: An electronic computing element which accepts a signal from a high-impedance source (e.g., a computing potentiometer) and furnishes a low-impedance output signal which is a function of the input signal. The functional relationship between the output and input signals is

$$e_o = R \sin K e_i$$

A dual sinusoid generator also supplies the output

$$e_o = R \cos K e_i$$

Class I: A computing element which requires the addition of one computing amplifier to meet the requirements for a Class 0 sinusoid generator.

Class II: A computing element which requires the addition of two computing amplifiers to meet the requirements for a Class 0 sinusoid generator.

Class III: A computing element which requires the addition of three computing amplifiers to meet the requirements for a Class 0 sinusoid generator.

VOLTAGE, MAXIMUM OUTPUT

The maximum stationary output voltage, either positive or negative, which can be delivered to a standard output load by a computing element without exceeding the static error.

METHODS OF MEASUREMENT

CURRENT, MAXIMUM INPUT

Servo Multiplier, Amplifier: The following circuit is recommended for measurement of maximum signal current required by the servo multiplier-amplifier.

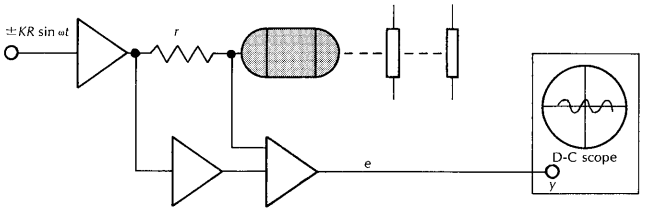


Figure M-1

Input current $= e/r$ $\quad K = .1, .5$ and 1

Recommended value of r is 100Ω

For any value of K, maximum input current is the peak value of e/r as ω is increased to the limit of the servo's ability to follow the input. The greatest of these currents is the maximum input current for the servo multiplier.

CURRENT, MAXIMUM OUTPUT

Maximum output current may be measured by using the circuit shown in the figure below. The comparator should be carefully selected for identical input

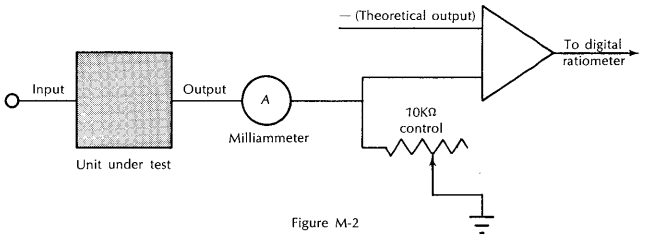


Figure M-2

The maximum output current for any output level is found by reducing the control resistance until the deviation between the actual output and its theoretical value is at the maximum specified value. The minimum found over the output range is the maximum output current of the element under test.

DRIFT

Arbitrary Electronic Function Generator: The circuit for measuring drift is shown below. Any change in output signal should be expressed in millivolts and as a percentage of R for input KR held constant for 9 hours. That value and polarity of KR which gives maximum drift should be used. The AEFG should be set up with the standard straight line function.

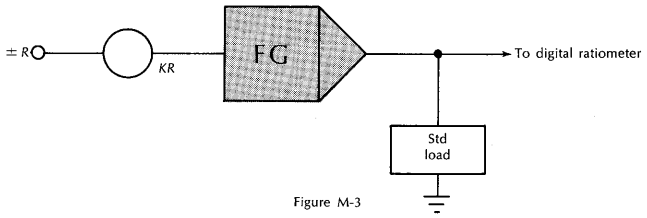


Figure M-3

Electronic Multiplier: The circuit for measuring drift is shown below. Any change in output signal should be expressed in millivolts and as a percentage of R for inputs K_1R and K_2R held constant for 9 hours. That value and polarity of K_1R and K_2R which gives maximum drift should be used.

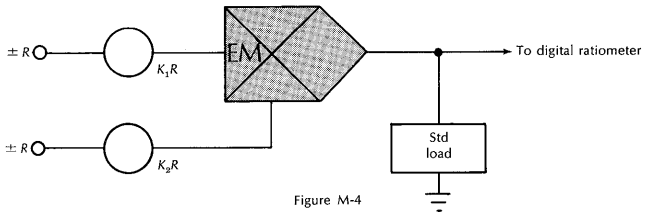


Figure M-4

Electronic Sinusoid Generator: The circuit for measuring drift is shown below. Any change in output signal should be expressed in millivolts and as a percentage of R for input KR held constant for 9 hours. That value and polarity of KR which gives the maximum drift should be used.

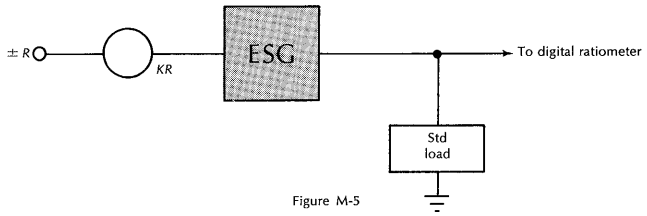


Figure M-5

Integrator Amplifier: The circuit for measuring drift is shown below. Drift should be measured for the following conditions:

TABLE OF CONDITIONS

Integrator Input to SJ (Summing Junction)	*Initial Condition*	*Computer Mode When Recording*
1. Unity gain grounded	Zero, $+R$, and $-R$	Hold, Operate
2. Standard input load	Zero, $+R$, and $-R$	Hold, Operate

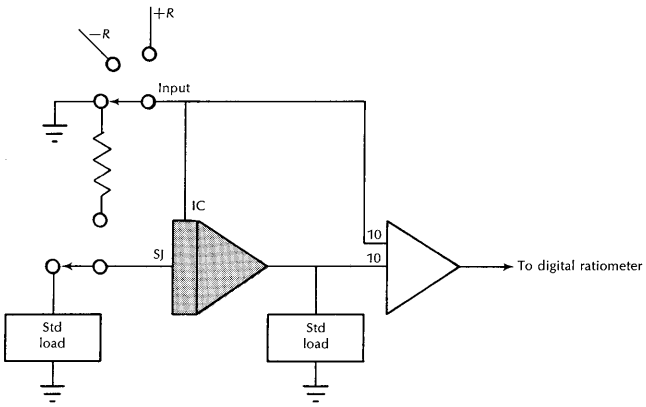


Figure M-6

To operate the above circuit, put the computer in the initial-condition mode for 3 or 4 minutes, thus permitting the capacitor to set to the proper initial value. Next, put the computer in the *operate* mode and record the output signal at intervals of 1, 10, and 100 minutes. Return the computer to the initial-condition mode for 3 or 4 minutes. Finally, put the computer to the *hold* mode and record the output signal after intervals of 1, 10, and 100 minutes. Repeat this process for each condition listed in the table above.

Servo Multiplier: The circuit for measuring drift is shown below. Any change in output signal should be expressed in millivolts, and as a percentage of *R* for input *KR* held constant for a period of 9 hours. That value and polarity of *KR* giving the maximum drift should be used.

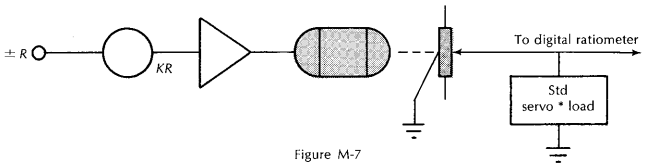


Figure M-7

Summing Amplifier: The circuit for measuring drift is shown below. Any change in output signal should be expressed in millivolts and as a percentage of *R* for input *KR* held constant for 9 hours. That value and polarity of *KR* which gives the maximum drift should be used.

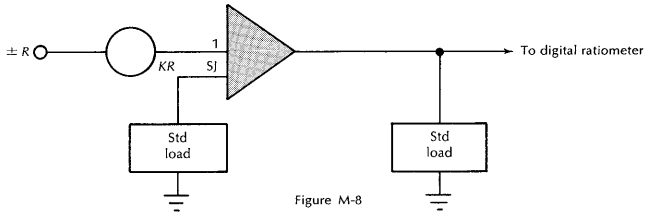


Figure M-8

*A standard servo load is the input impedance of an operational amplifier with unity gain.

ERROR, SETUP

Arbitrary Electronic Function Generator: The function shown in Figures M-9 and M-10 are suitable for measuring the setup errors in function generators.

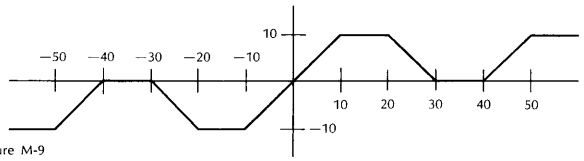


Figure M-9

As indicated in Figure M-9, all slopes should be set to + or − one with the pattern extended to cover the entire range available on the *x*-axis. The error is the departure from the ideal output for a stationary input and should be expressed in millivolts and percent of *R*.

The function generator should then be reset to conform to Figure M-10 and the same measurements of error taken for this case.

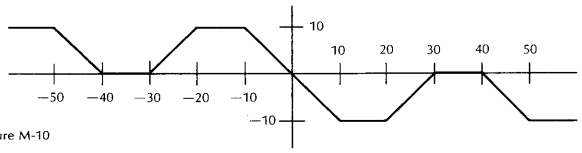


Figure M-10

Various types of setup procedure shall be considered as follows:

1. Set up by hand while observing null meters. After standard setup, measure departure by means of a digital voltmeter. The function set up in this manner can have discrepancies due to failure of diodes to conduct at the actual breakpoint value or due to meter or calibration-setup-potentiometer inaccuracies.
2. Set up by servo push-button. After standard setup, measure departure from desired function by means of a digital voltmeter. The function can have discrepancies due to servo null or drift and/or errors in the voltage divider reference. Also, failure of diodes to conduct at set values can cause errors.
3. Set up by tape program. Punch tape according to desired function. After standard setup, measure departure by means of a digital voltmeter.
4. Set up by card insert. Punch card according to desired function. After inserting card, measure departure from desired function by means of a digital voltmeter. The function can have discrepancies due to errors in breakpoint or slope resistors, mechanical malfunction, or failure of diodes to conduct at set values.

Since all errors are not necessarily cumulative, measurements should be made at discrete intervals along the test curves.

ERROR, TOTAL

Electronic Multiplier: The following procedure is suggested for measuring and plotting total error as a function of frequency. The maximum error at each frequency may be measured by generating functions defined by plane-surface intersections of the error surface.

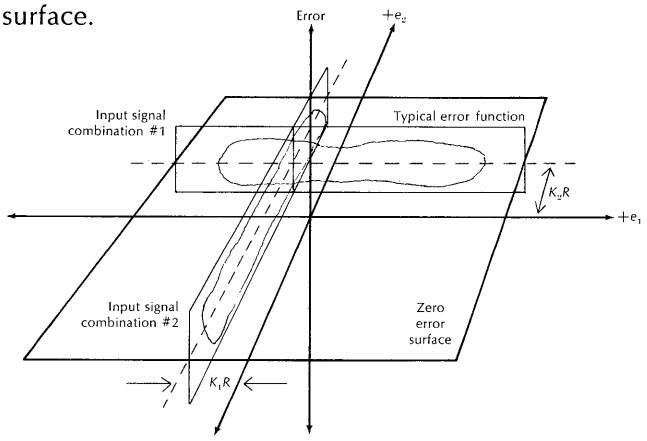


Figure M-11

These error functions should be obtained for the following input signal combinations:

1. $e_1 = K_1R \sin \omega t, -K_2R \leq e_2 \leq K_2R \quad K_1 = 1$ and .01
2. $e_2 = K_1R \sin \omega t, -RK_2 \leq e_1 \leq K_2R \quad 0 \leq K_2 \leq 1$

Values of e_1 and e_2 in the range shown which yield the greatest error should be used. The maximum peak error resulting from any combination is the value to be used in plotting the error-vs.-frequency curve, an example of which is shown below. Curves should be shown for each of the suggested values of K_1.

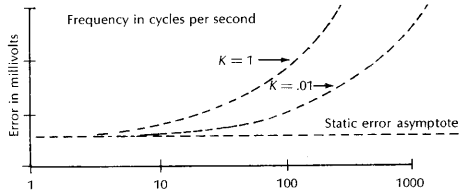


Figure M-12

The circuit diagram below yields error functions for input condition #1. Error functions for input condition #2 are obtained by reversing the inputs e_1 and e_2.

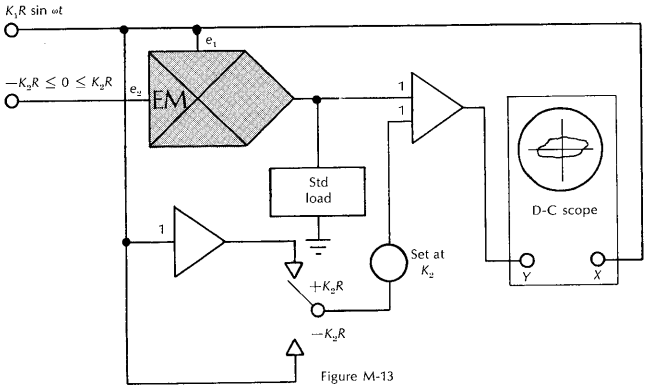


Figure M-13

The potentiometer setting is maintained at K_2.* Highest precision potentiometer setting techniques should be used.

Servo Multiplier: Total error may be measured by means of the circuit shown below, and plotted as a function of frequency. A family of curves should be obtained for K values of 1, .5, .2, .1, .05, and .005. All ganged potentiometers should be excited with $\pm R$, and the greatest errors occurring in the system should be plotted.

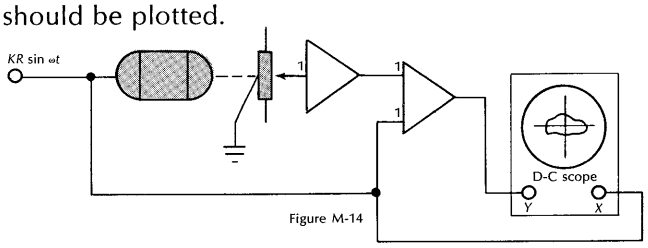


Figure M-14

If servo feedback is variable, additional curves should be plotted for discrete values of feedback voltage over the entire prescribed range.

A typical total-error plot for one specific feedback voltage condition is shown below.

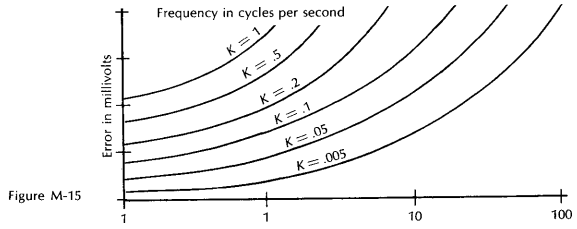


Figure M-15

Summing Amplifier: Total error may be measured by using the setup shown in the figure below. The comparator should be carefully selected so that the input impedances are identical in value.

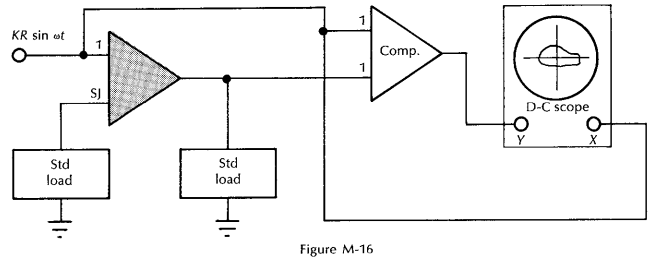


Figure M-16

A typical result for the suggested value of K, is shown below.

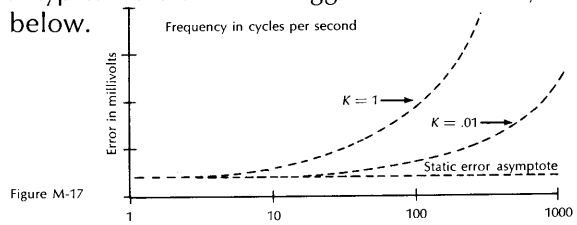


Figure M-17

*For wide-band multipliers, a phase-compensated potentiometer may be required; alternatively, a potentiometer with a resistance as low as possible, consistent with the amplifier's current output capability, may be used to minimize phase shift.

FREQUENCY RESPONSE, AMPLITUDE

Amplifier: The following circuit is recommended for measurement of amplifier frequency response (amplitude):

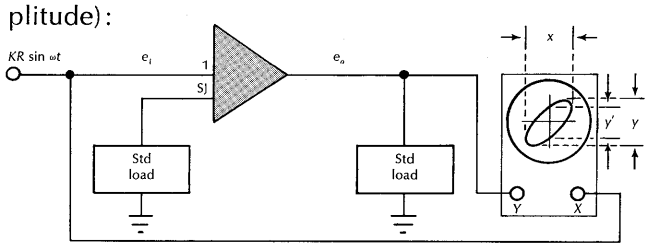


Figure M-18

$$\text{Amplitude ratio} = \frac{\text{modulus } e_o}{\text{modulus } e_i} = \frac{y}{x}$$

Suggested values of *K* are 0.01 and 1.0

Plot amplitude ratio on 8½" x 11", 3-cycle semilog graph paper. Plot over frequency range of 1 to 1000 cps and 1000 to 1,000,000 cps.

Arbitrary Electronic Function Generator: The following circuit is recommended for measurement of function generator frequency response (amplitude):

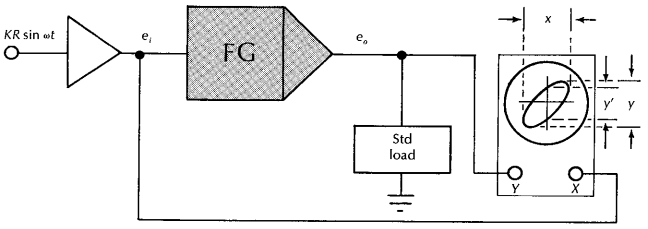


Figure M-19

$$\text{Amplitude ratio} = \frac{\text{modulus } e_o}{\text{modulus } e_i} = \frac{y}{x}$$

Suggested values of *K* are 0.01 and 1.0.

The following function is to be used for this test:

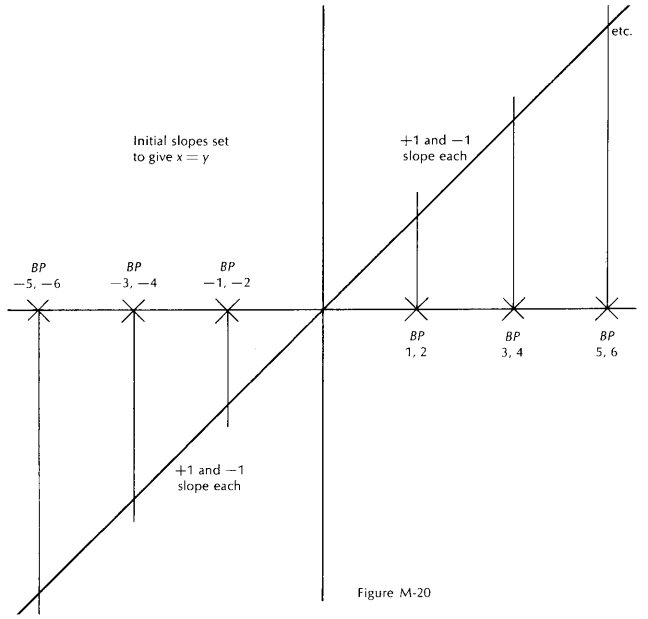


Figure M-20

Note that all breakpoints are used and are paired at equal intervals over the input range. A unity negative and positive slope is set in at each point except at the origin. This should result in a line straight enough for frequency response tests. The initial ± slopes are to be adjusted so as to give a total line slope of one, so that x = y. In the case of fixed breakpoint function generators, it will be necessary to interchange components with another function generator to allow the pairing of breakpoints.

Plot amplitude ratio on 8½" x 11", 3-cycle, semilog graph paper over frequency range of 1 to 1000 cps, or more if desired.

Electronic Multiplier: The following circuit is recommended for measurement of electronic multiplier frequency response (amplitude):

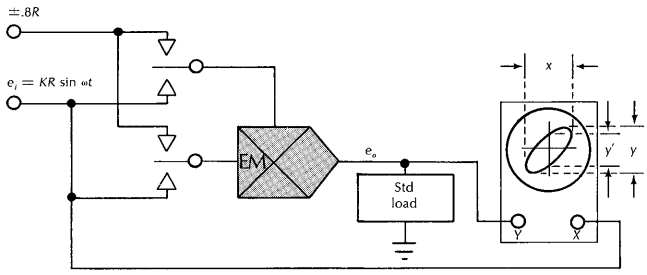


Figure M-21

$$\text{Amplitude ratio} = \frac{\text{modulus } e_o}{\text{modulus } e_i} = \frac{y}{x}$$

Suggested values of *K* are 0.01 and 1.0

Input signals should be permuted through the two inputs. Plot only that combination of inputs giving greatest deviation each for ±.8*R*.

Plot on 8½" x 11", 3-cycle semilog graph paper over frequency range of 1 to 1000 cps.

Electronic Sinusoid Generator: The following circuit is recommended for measurement of electronic sinusoid generator frequency response (amplitude):

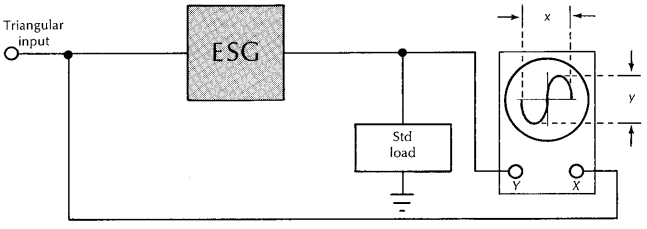


Figure M-22

Use a triangular wave of sufficient amplitude to drive the electronic sinusoid generator over its full range (±180°). Plot the output amplitude-vs.-frequency on 8½" x 11", 3-cycle semilog graph paper over a frequency range of 1 to 1000 cps. One cps on the triangular function generator = 2 cps on the log plot. Use a triangular wave to drive the electronic

sinusoidal generator over ±.01 *R* peak to peak, and plot results as above.

Servo Multiplier: The following circuit is recommended for measurement of servo multiplier frequency response (amplitude):

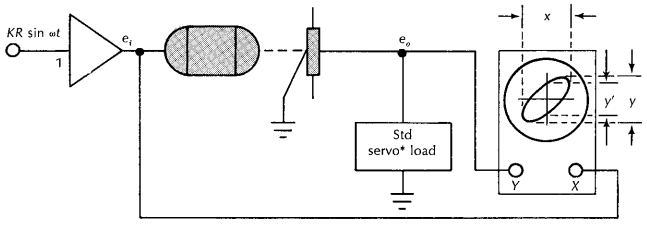


Figure M-23

$$\text{Amplitude ratio} = \frac{\text{modulus } e_o}{\text{modulus } e_i} = \frac{y}{x}$$

R = value of reference voltage

Suggested values of K are 1.0, .5, .2, .1, .05, and .005.

Plot amplitude ratio on 8½" x 11", 3-cycle semi-log graph paper over frequency range of 0.1 to 1000 cps for each value of e_i.

If servo feedback voltage is variable, plot response at discrete values of feedback voltage over entire range of prescribed feedback voltage. (Set damping, if variable, at recommended value.)

FREQUENCY RESPONSE, PHASE

Amplifier: The circuit used for measurement of amplifier frequency response (amplitude) is suitable also for measuring phase shift, α.

$$\sin \alpha = y'/y$$

where y' is the distance between y-axis intercepts by the Lissajous figures. Phase angle may be plotted on the same graph as amplitude and over the same frequency range.

An alternative method for measuring phase shift involves the use of a time interval meter. Set the counter trigger at zero on positive slope for both inputs, e_i and e_o. Extreme care should be taken in the setting of the trigger levels.

$$\text{Phase shift } \alpha \text{ (degrees)} = (t/T) \times 360$$

where t = reading in seconds on the counter
T = period of sine wave

Arbitrary Electronic Function Generator: The circuit used for measurement of function-generator frequency response (amplitude) is suitable also for measuring phase shift.

$$\sin \alpha = y'/y$$

where y' is the distance between y-axis intercepts by the Lissajous figure. Phase angle may be plotted on the same graph as amplitude and over the same frequency range.

*A standard servo load is the input impedance of an operational amplifier with unity gain.

An alternative method for measuring phase shift involves the use of an electronic counter. Set the counter trigger at zero on positive slope for both inputs, e_i and e_o.

$$\text{Phase shift } \alpha \text{ (degrees)} = (t/T) \times 360$$

where t = reading in seconds on the counter
T = period of sine wave.

Electronic Multiplier: The circuit used for measurement of multiplier frequency response amplitude is suitable also for measuring phase shift.

$$\sin \alpha = y'/y$$

where y' is the distance between y-axis intercepts by the Lissajous figure. Phase angle may be plotted on the same graph as multiplier amplitude response and over the same frequency range.

Input signals should be permuted through the two multiplier inputs. Plot the same combination of inputs as plotted in amplitude response measurements.

An alternative method for measuring phase shift involves the use of an electronic counter. Set the counter trigger at zero on positive slope for both inputs, e_i and e_o.

$$\text{Phase shift } \alpha \text{ (degrees)} = (t/T) \times 360$$

where t = reading in seconds on the counter
T = period of sine wave.

Electronic Sinusoid Generator: The circuit used for measurement of electronic sinusoid generator frequency response (amplitude) is suitable also for measuring phase shift, except that the oscilloscope is replaced with an electronic counter. For the sine input, both channels of the counter should be set to trigger at zero on positive slopes. For the cosine input, compare phase with the sine, and add or subtract figure previously obtained for sine to 90 degrees.

$$\text{Phase shift } \alpha \text{ (degrees)} = (t/T) \times 360 \times 2 \text{ triangular wave frequency}$$

where t = reading in seconds on counter
T = period of triangular wave

Servo Multiplier: The circuit used for measurement of servo frequency response (amplitude) is suitable also for measuring phase shift.

$$\sin \alpha = y'/y$$

where y' is the distance between y-axis intercepts by the Lissajous figure. Phase angle may be plotted on the same graph as amplitude and over the same frequency range.

If necessary, vary feedback voltage and damping as described in measurement of amplitude response.

An alternative method for measuring phase shift involves the use of an electronic counter. Set the counter trigger at zero on positive slope for both inputs, e_i and e_o.

Phase shift α (degrees) $= (t/T) \times 360$

where $t =$ reading in seconds on the counter
$T =$ period of sine wave.

NOISE

Arbitrary Electronic Function Generator, Electronic Multiplier, Electronic Sinusoid Generator, Summing Amplifier: Circuits for measuring the noise of the above components are shown below. Results should be given in photo-oscillograms with y-axis calibrations in peak-to-peak millivolts and as a percentage of *R*.

Description of Filter

The filter shown in the noise measuring circuits consists of a resistor and capacitor as shown below.

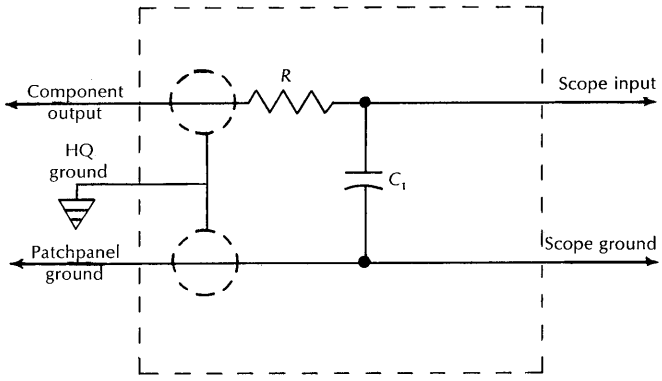


Figure M-24 Noise filter

The results given should be for filter cutoff frequencies of 79.5, 795, 7,950 and 79,500 cps. The resistor and capacitor of the filter should be in a well-shielded box to minimize 60-cycle pickup.

Input impedance of the oscilloscope and associated wiring should be at least 1 megohm with less than 200 pf shunt capacity. Attenuation of the filter is about 6 db/octave above cutoff. With the resistor value at 2*K* ohms, the capacitor values for the cutoff frequencies are as follows:

Frequency	*Capacitor Value*
79.5 cps	1.0 mfd
795 cps	0.1 mfd
7,950 cps	0.01 mfd
79,500 cps	0.001 mfd

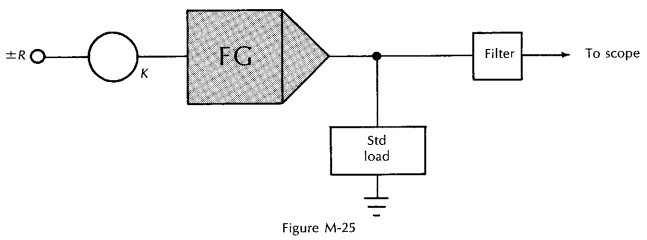


Figure M-25

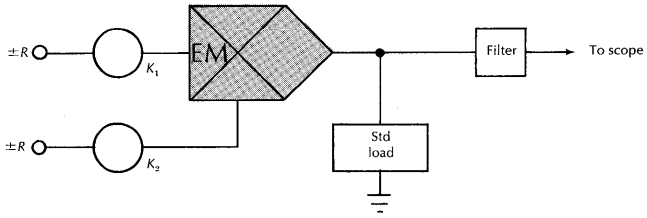


Figure M-26

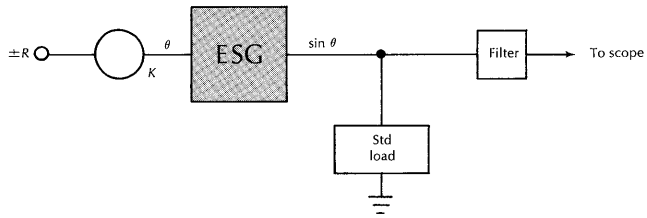


Figure M-27

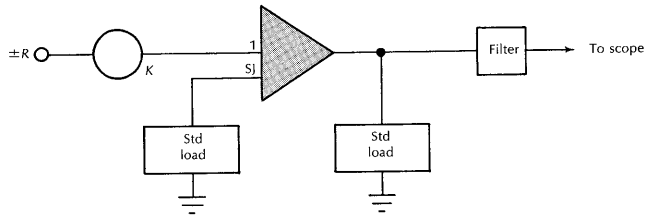


Figure M-28

RECOVERY TIME, OVERLOAD

Arbitrary Electronic Function Generator, Electronic Multiplier, Electronic Sinusoid Generator, Summing Amplifier: Circuits for measuring the overload recovery time are shown below. The test should be made by applying the input(s) indicated. The polarity of input giving the longest recovery time should be used. Results should be given in photo-oscillographs with *X*-axis calibrations in time. Employ double silicon diodes as shown to allow sufficient oscilloscope gain without overloading the oscilloscope amplifier. Oscilloscope *Y* amplifier should be direct-coupled, *i.e.*, on D-C

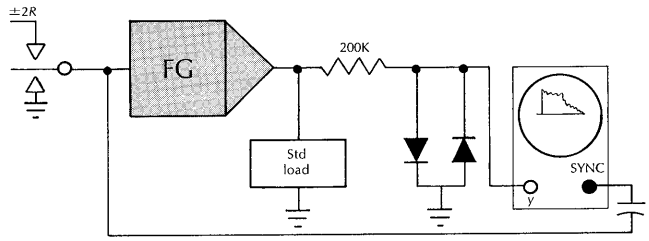


Figure M-29

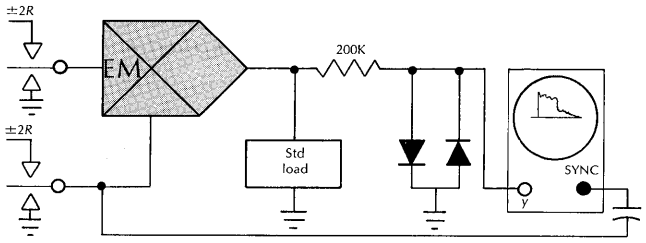


Figure M-30

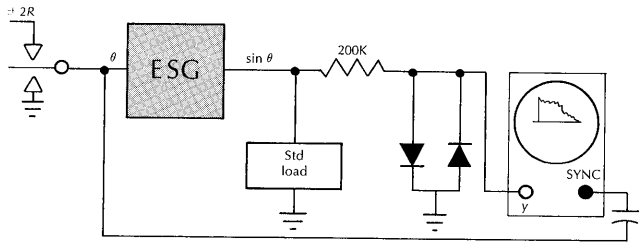


Figure M-31

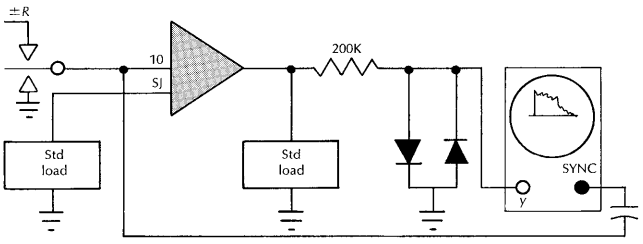


Figure M-32

RESPONSE, TRANSIENT

Arbitrary Electronic Function Generator: A circuit suitable for measuring transient response is shown below. The function generator should be set up to the standard straight-line curve as recommended under the section on amplitude response measurement.

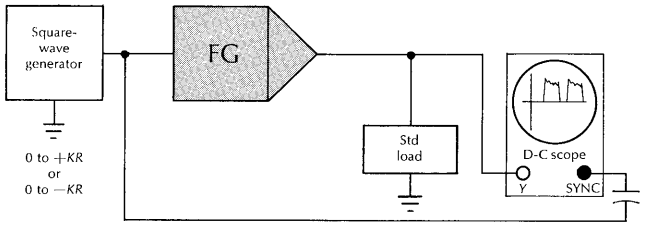


Figure M-33

Photo-oscillograms of the results should be given for K equal to 0.1 and 0.8. Square-wave frequency and oscilloscope timing should be adjusted to provide a clear display of any tendency to ring.

The circuit recommended for square-wave generation is shown separately.

Electronic Multiplier: The circuit arrangement shown below is intended for the measurement of transient response of electronic multipliers.

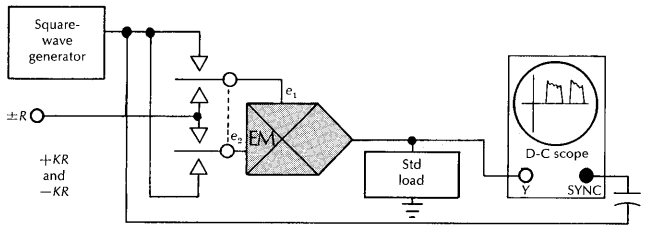


Figure M-34

A photo-oscillogram of the results for the worst combination of inputs and sign of K should be given. Suggested values of K are .1 and 1.0. Square-wave frequency and oscilloscope timing should be adjusted to provide a clear display of any tendency to ring. A recommended circuit for square-wave generation is shown separately.

Electronic Sinusoid Generator: The transient response of this unit may be measured by means of the circuit shown below.

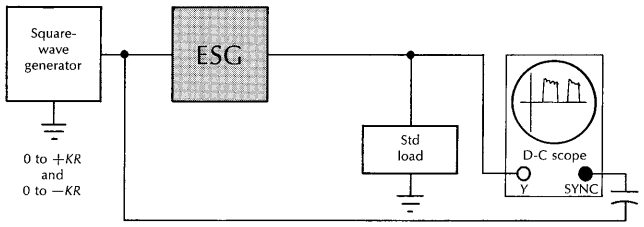


Figure M-35

Suggested values of K are .8 and .1

Photo-oscillograms should be made for both values and both signs of KR. Square-wave frequency and oscilloscope timing should be adjusted for optimum presentation of any tendency to ring. The circuit for square-wave generation is shown separately.

Servo Multiplier: Transient response of the servo-multiplier may be measured by means of the circuit shown below.

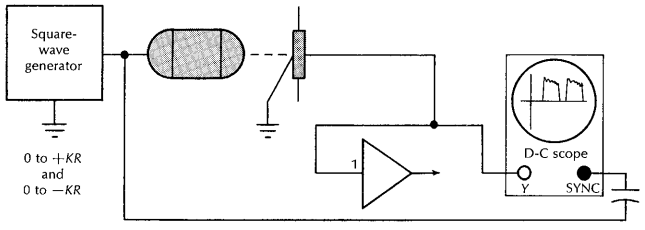


Figure M-36

Suggested values of K are .8, .1, and .005

Photo-oscillograms should be made for each of the values of 0 to $+KR$ and 0 to $-KR$ indicated. If the servo gain is adjustable, the test should be made for both extremes of adjustment as well as the optimum setting. Square-wave frequency and oscilloscope timing should be adjusted for optimum

presentation of any tendency to ring. The circuit recommended for square-wave generation is shown separately.

Summing Amplifier: Transient response may be measured by means of the circuit diagram shown below. Results should be shown as a photo-oscillogram of the output signal *vs.* time.

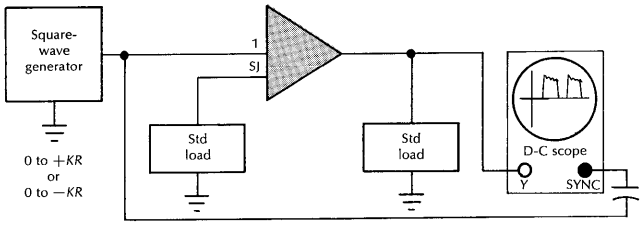


Figure M-37

Output of the square-wave generator should be 0 to $+KR$ and 0 to $-KR$, where the recommended values of K are .1 and 1.0. The frequency of the square wave, and the time scale of the oscilloscope sweep, should be adjusted to give a clear display of any tendency to ring. A suggested circuit for square-wave generation is shown separately.

RESPONSE, TRANSIENT, UNDER CAPACITIVE LOADING

Summing Amplifier: Tolerance to capacitive loading should be measured by means of the setup below over the range of capacitances and resistances shown.

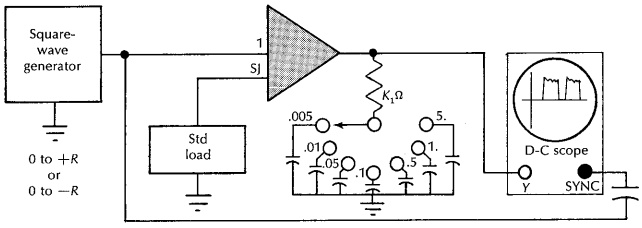


Figure M-38

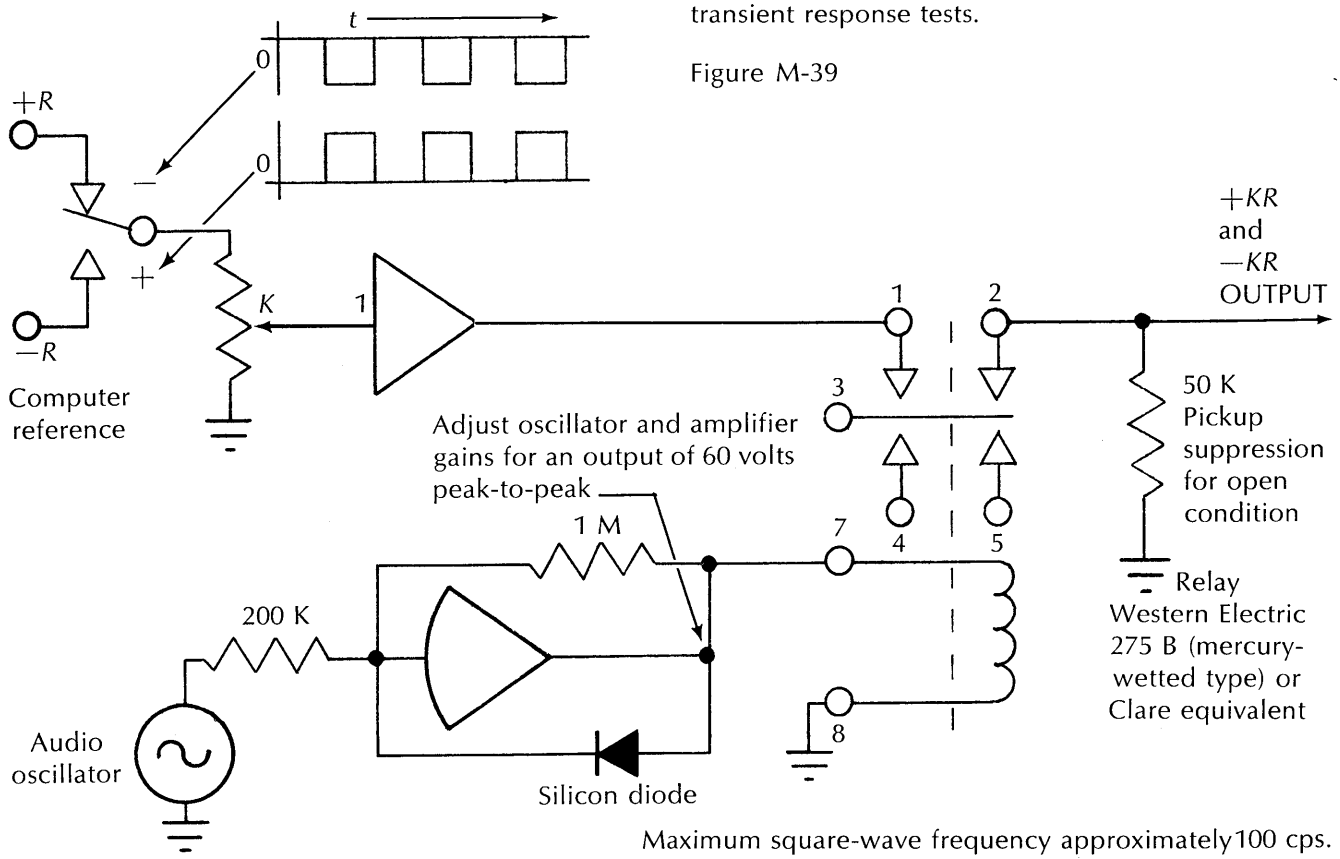
Suggested values of K_1 are 1, 100, 1,000, and 10,000 Ω

The sign of R resulting in the greatest error should be shown by means of photo-oscillograms. Square-wave frequency and oscilloscope timing should be adjusted to give a clear display of any tendency to ring. The circuit recommended for square-wave generation is shown separately.

SQUARE-WAVE GENERATOR

The following arrangement will provide the high output-voltage levels and fast rise-times required for transient response tests.

Figure M-39



Maximum square-wave frequency approximately100 cps.